EE 505

Lecture 22

ADC Design

- Multi-Step Flash
- Pipeline

Review from Last Lecture

What Architectures are Actually Used

DACs
Texas Instruments Mar 1, 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

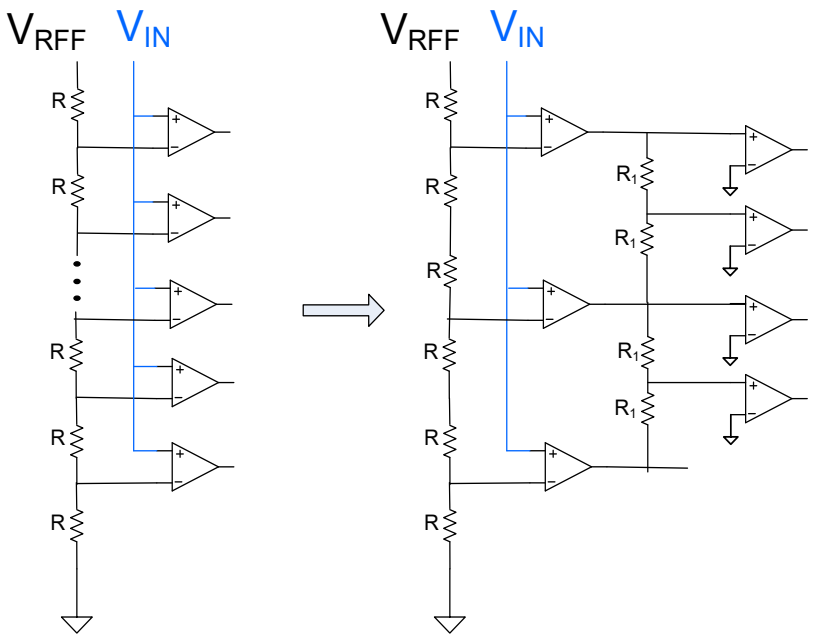
ADCs
Texas Instruments April 13 2023

SAR	728
Pipeline	294
Delta Sigma	187
Folding Interpolating	66
Delta Sigma Modulator	9
Two-Step	6
Flash	3
Total	1293

- These are catalog parts
- Specific details about architecture usually absent in data sheets
- Some (many) in list are slight variants and carry different part numbers
- Variety of converters used in ASIC applications will be larger

Review from last lecture

Interpolating Flash ADC



Standard Flash

Interpolated Flash

- Reduction in pre-amp area and power
- Latches all referenced to ground
- Loading on V_{IN} reduced
- Kickback to V_{REF} reduced
- V_{IN} coupling to V_{REF} reduced
- Multiple levels can be included in interpolator array

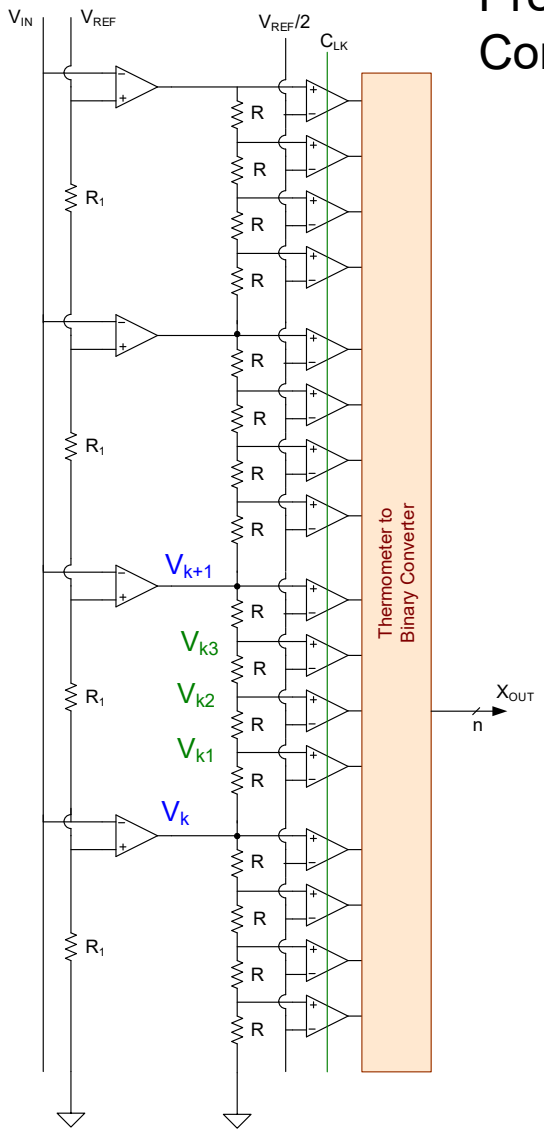
Review from last lecture

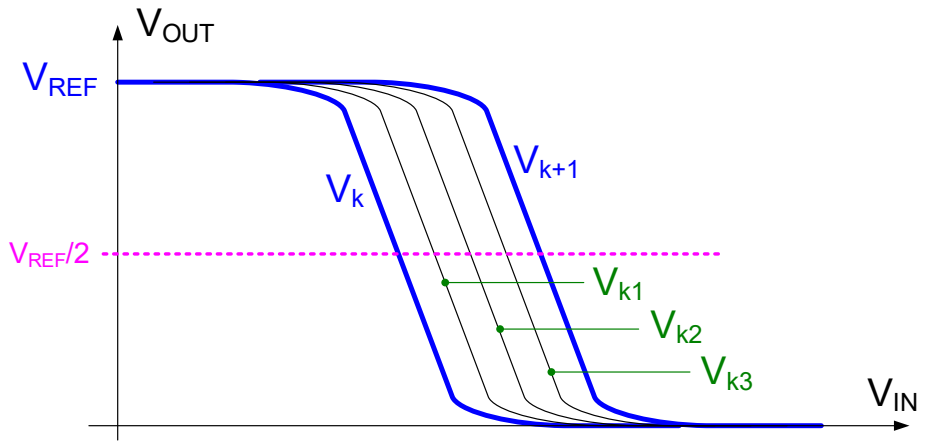
Interpolating Flash ADC

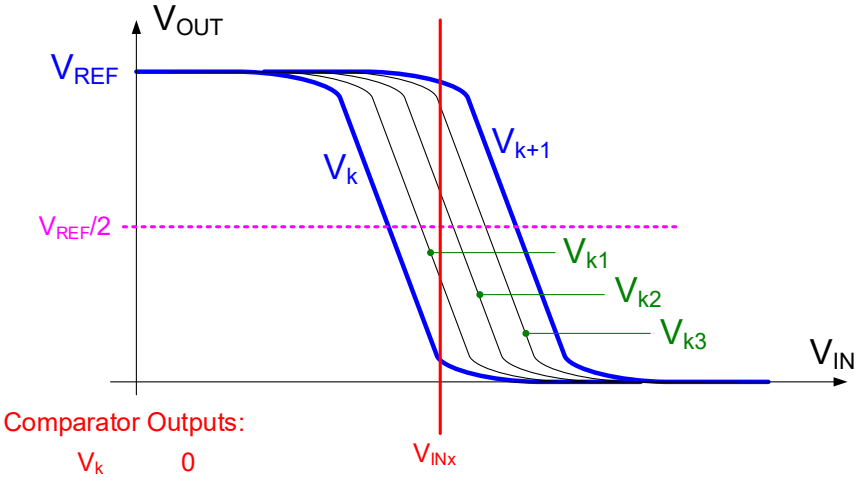
4 –levels of interpolation

Preamp gain not critical

Common mode set at $V_{REF}/2$







Comparator Outputs:

V_k	0
V_{k1}	0
V_{k2}	1
V_{k3}	1
V_{k+1}	1

Review from last lecture

Flash ADC Summary

Flash ADC

Very fast

Simple structure

Usually Clocked

Bubble Removal Important

Seldom over 6 or 7 bits of resolution

- Flash ADC has some really desirable properties (simple and fast)
- Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

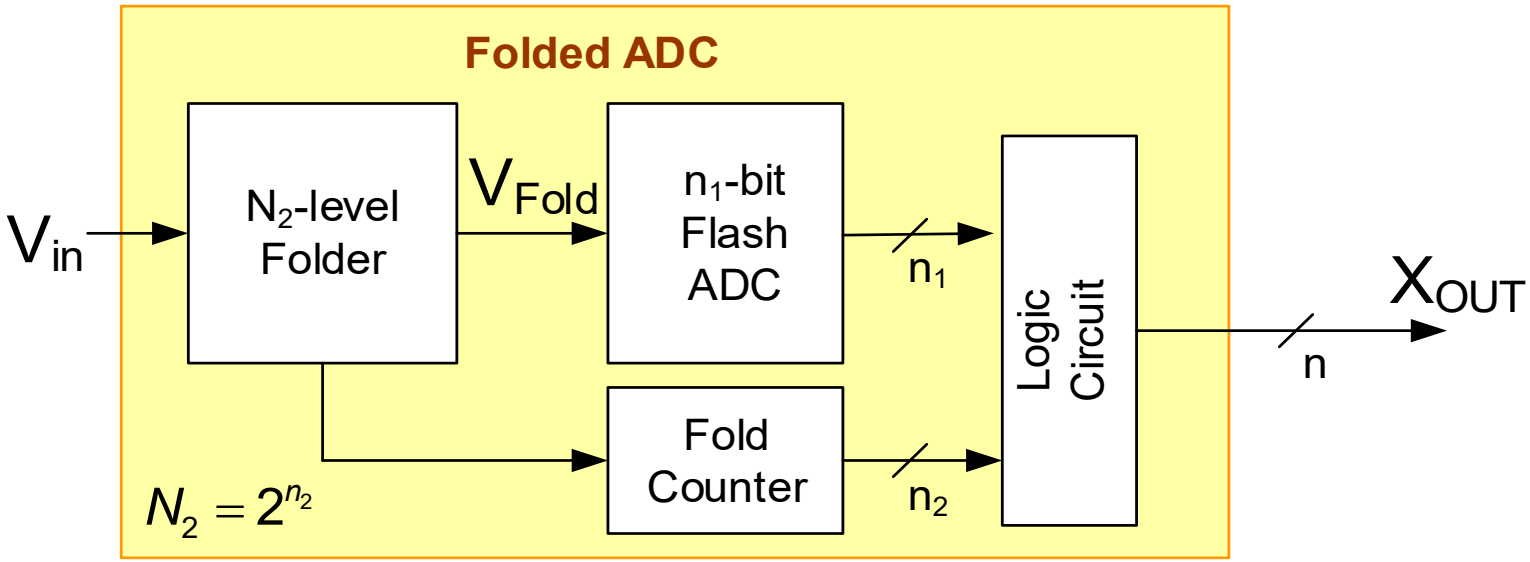
To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

- **Number of comparators increases geometrically --- 2^n**
- **String DAC area increases geometrically**
- **Too many comparators making non-critical decisions increases power**

Review from last lecture

Folded ADC Architecture



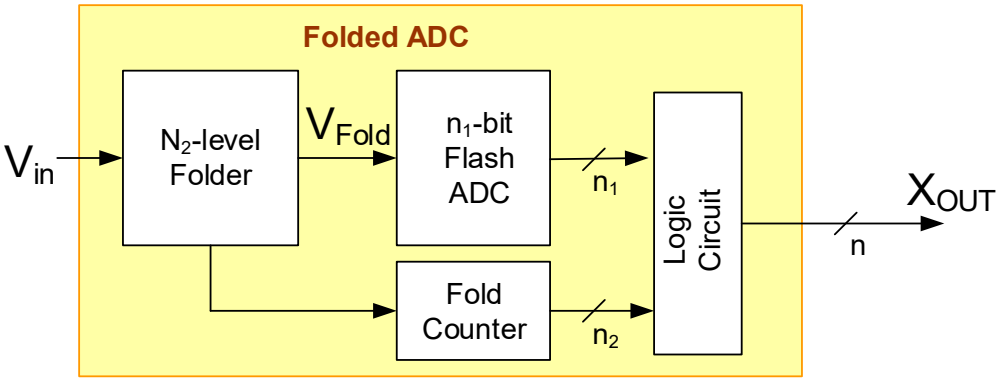
Premise: Folder provides large gain and is very fast

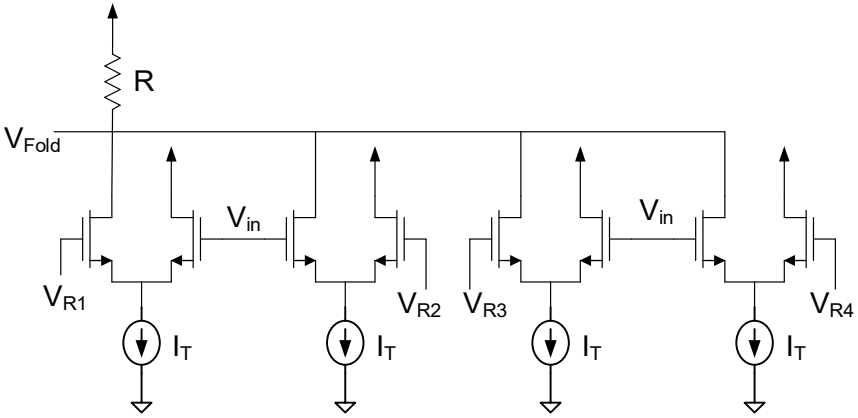
Similar in concept to interpolating flash ADC but

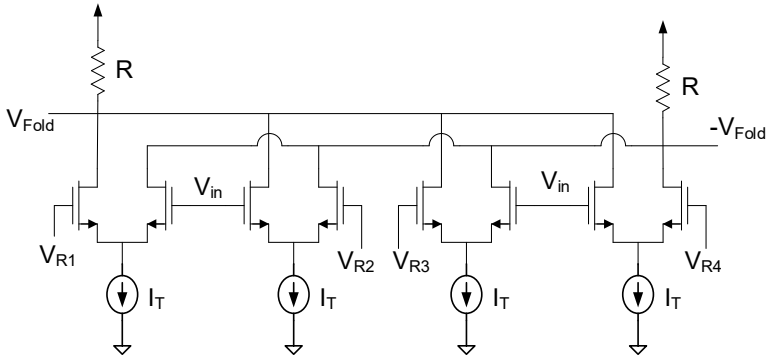
- Number of comparators has been reduced
- Thermometer to Binary decoder is eliminated

Review from last lecture

Folded ADC Architecture



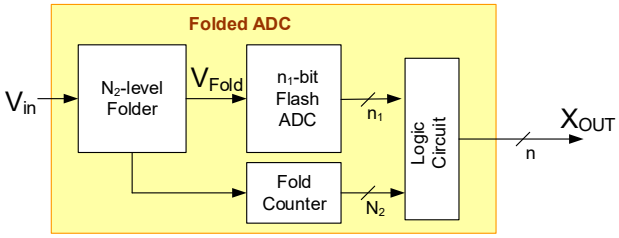




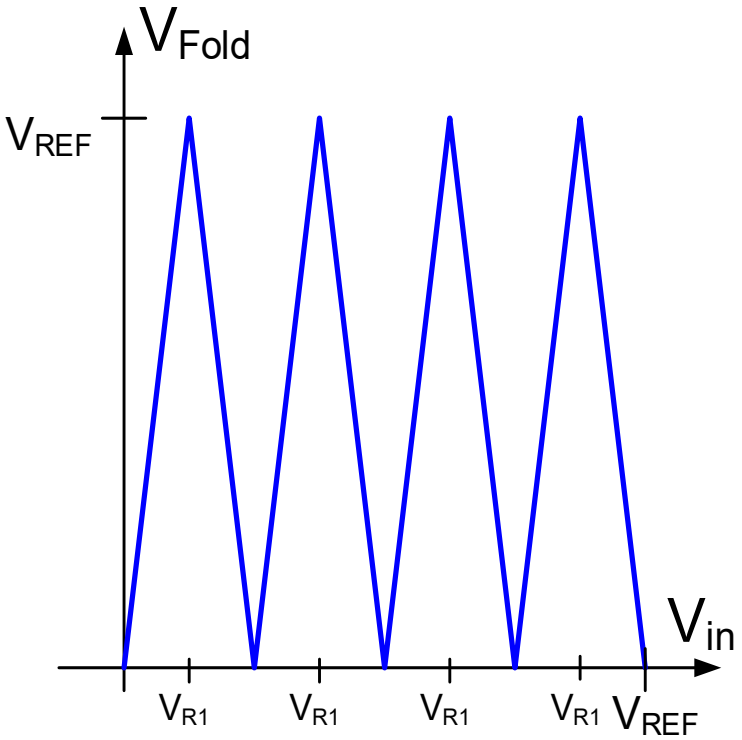
- Usually implemented in differential form
- Differential output almost free

Review from last lecture

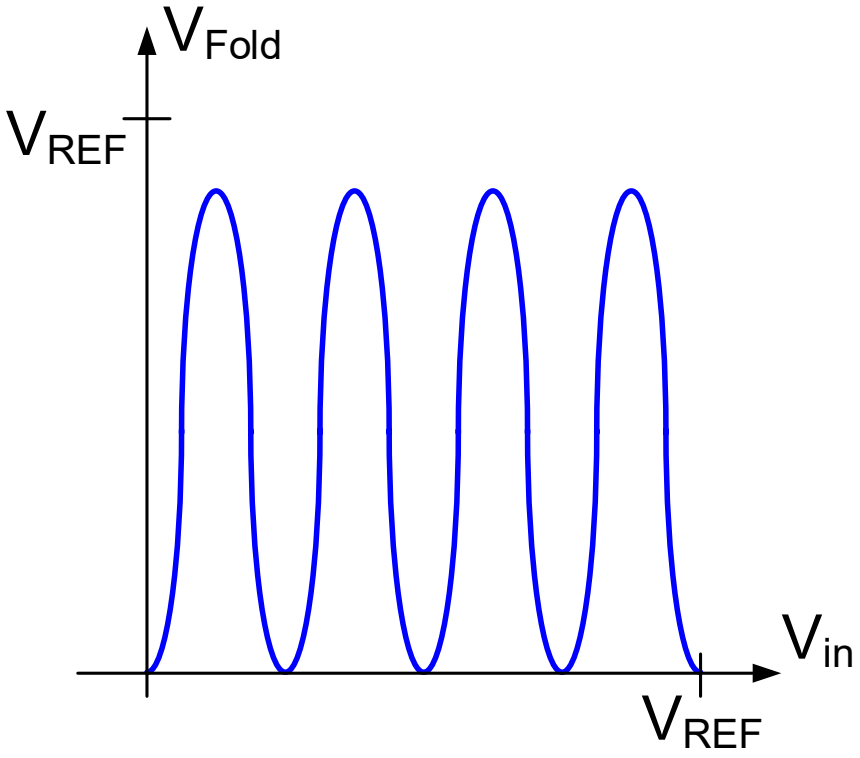
Folded ADC Architecture



Ideal Folder



Typical Folder



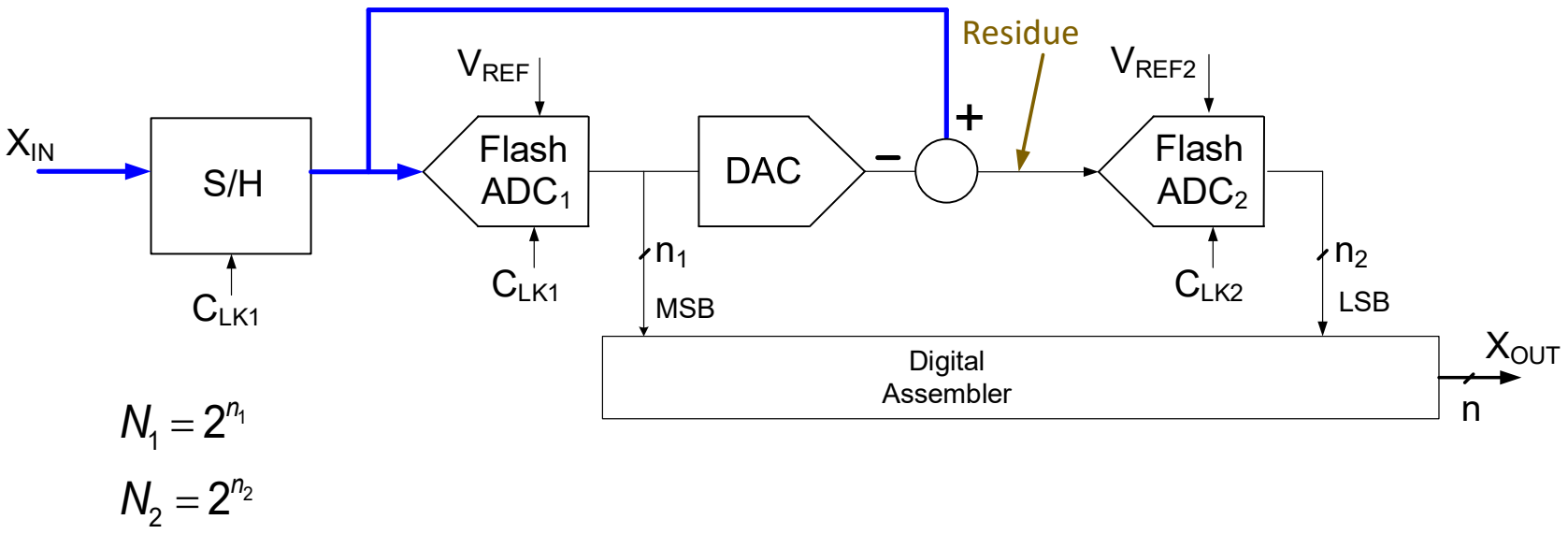
Nonlinearity in folder not a major problem since resolution nonlinearity affects primarily the LSBs and resolution of folded ADCs not large

Multi-Step Flash Approaches

Goal with Multi-Step Flash Approach:

- Reduce number of comparators and sub DAC levels
- Reduce or eliminate un-necessary comparator decisions

Two-Step Flash ADC



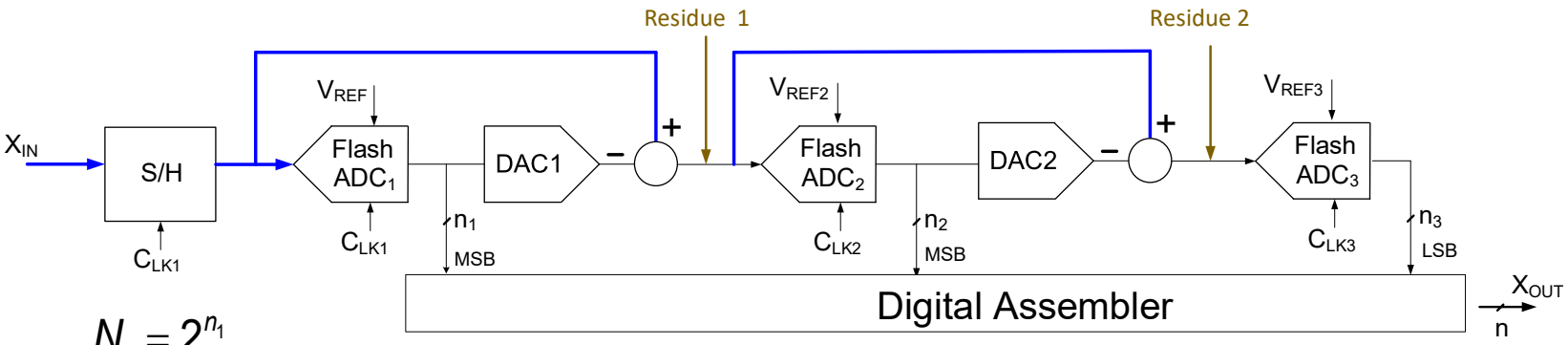
$N_1 = 2^{n_1}$

$N_2 = 2^{n_2}$

- Can operate asynchronously after S/H
- If clocked, C_{LK2} must be delayed from C_{LK1}
- Full-range of Residue signal is V_{REF}/N_1
- Reduces number of comparators from $2^{n_1+n_2}$ *to* $2^{n_1} + 2^{n_2}$
- V_{REF2} can be reduced by a factor of N_1 from V_{REF}

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1
- DAC accuracy and difference amplifier performance important

Three-Step Flash ADC



$$N_1 = 2^{n_1}$$

$$N_2 = 2^{n_2}$$

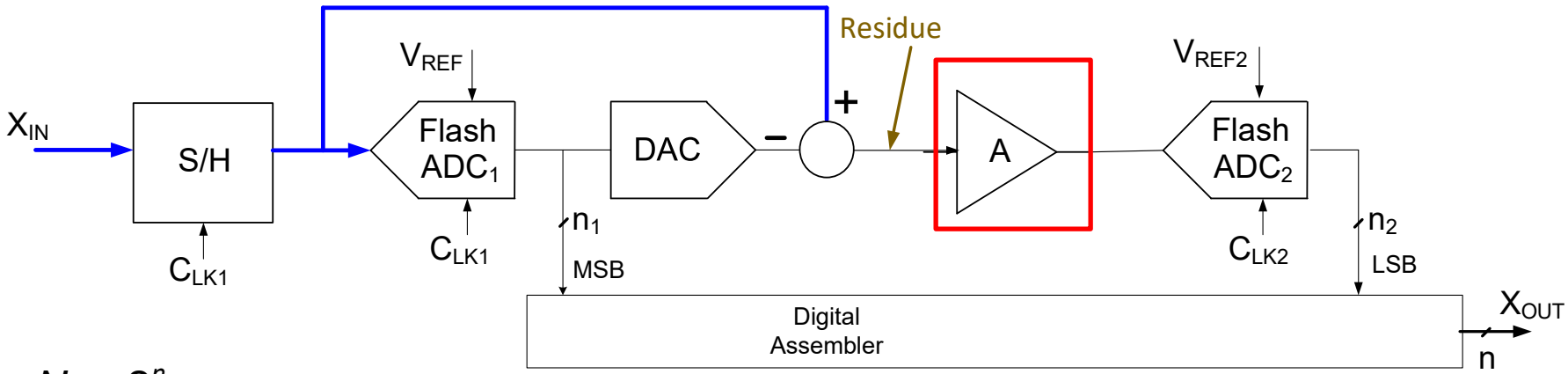
$$N_3 = 2^{n_3}$$

- Can operate asynchronously after S/H
- Full-range of Residue 2 signal is $V_{REF}/(N_1N_2)$
- Reduces number of comparators by factor from
- V_{REF3} can be reduced by a factor of N_2 from V_{REF2} $2^{n_1+n_2+n_3}$ *to* $2^{n_1}+2^{n_2}+2^{n_3}$

- No improvement in offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1

– DAC accuracy and difference amplifier performance important
– Complexity appears to be increasing

Two-Step Flash ADC with Interstage Gain

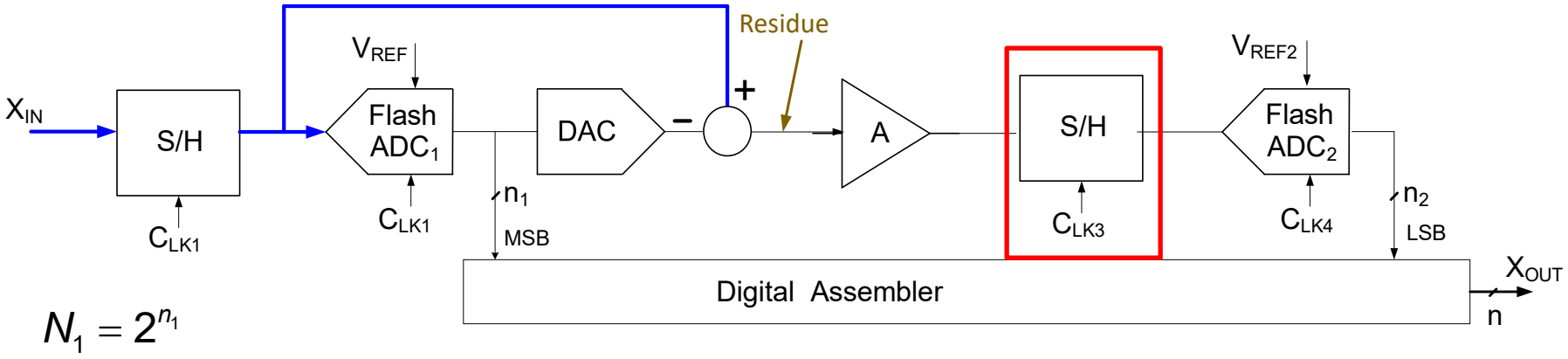


$N_1 = 2^{n_1}$

- A is typically N_1
- Dramatic reduction on offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1

– DAC accuracy and difference amplifier performance important
– Amplifier accuracy and linearity important
– Speed and power degrade due to A amplifier and diff amplifier
– Complexity appears to be increasing even more !!

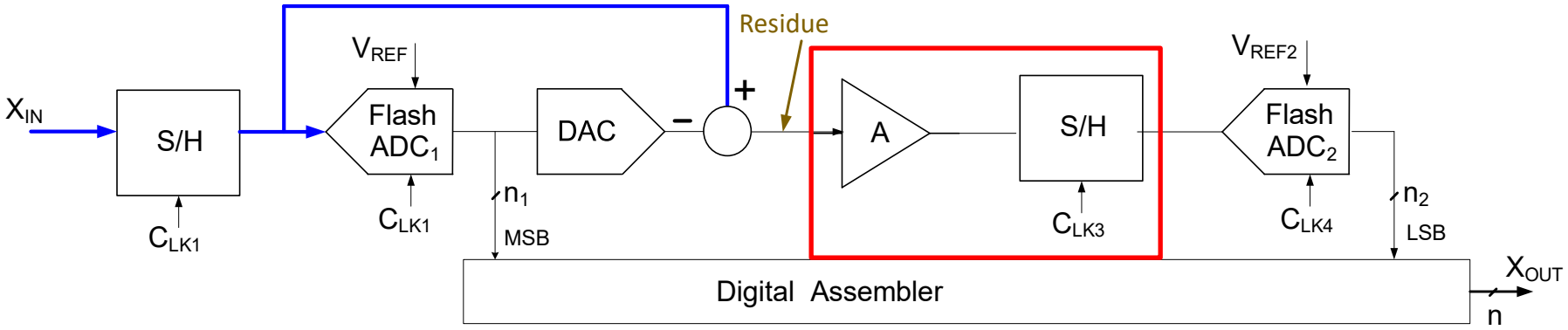
Two-Step Flash ADC with Interstage Gain and S/H



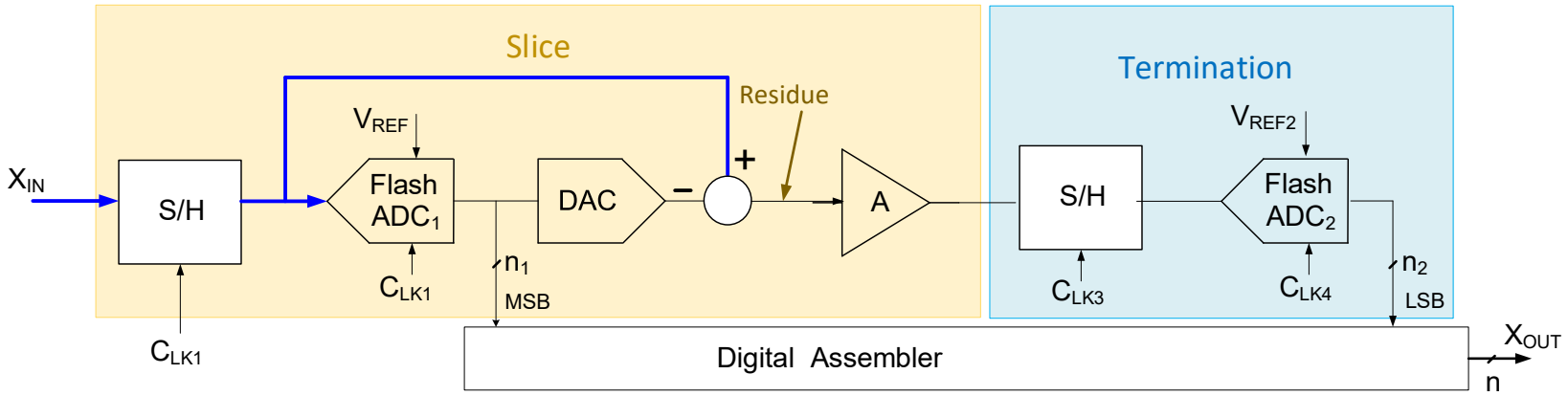
- Second S/H eliminates need to keep output of first block constant when Flash ADC_2 operates
- A is typically N_1
- Dramatic reduction on offset requirements on comparators of second-stage flash
- Common-mode signal swing on comparators in second-stage flash reduced by factor of N_1

– DAC accuracy and difference amplifier performance important
– Amplifier accuracy and linearity important
– Speed and power degrade due to A amplifier and diff amplifier
– Speed and accuracy degrade due to S/H
– Complexity appears to be increasing even more !!!

Two-Step Flash ADC with Interstage Gain and S/H

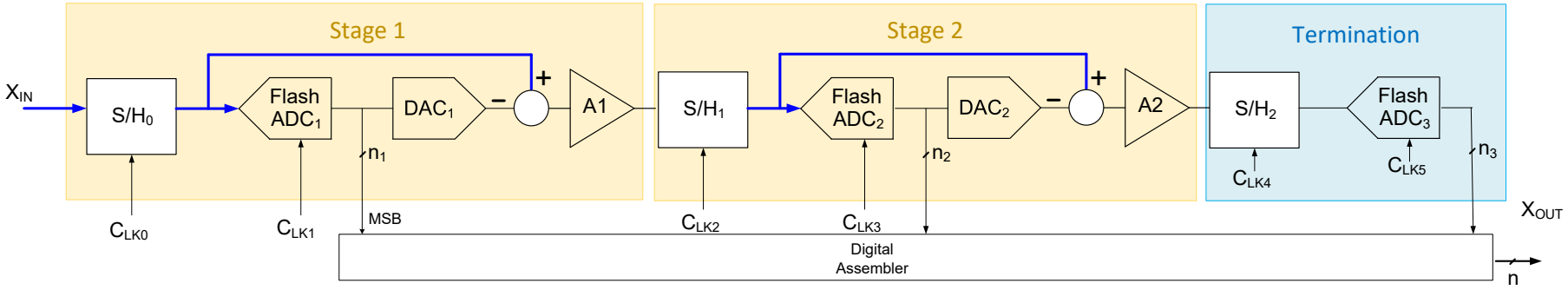


Slice can be repeated to obtain three-step Flash ADC



If limitations can be mitigated, further reduction in comparators with 3-step approach

Three-Step Flash ADC with Interstage Gain and S/H



$$N_1 = 2^{n_1}$$

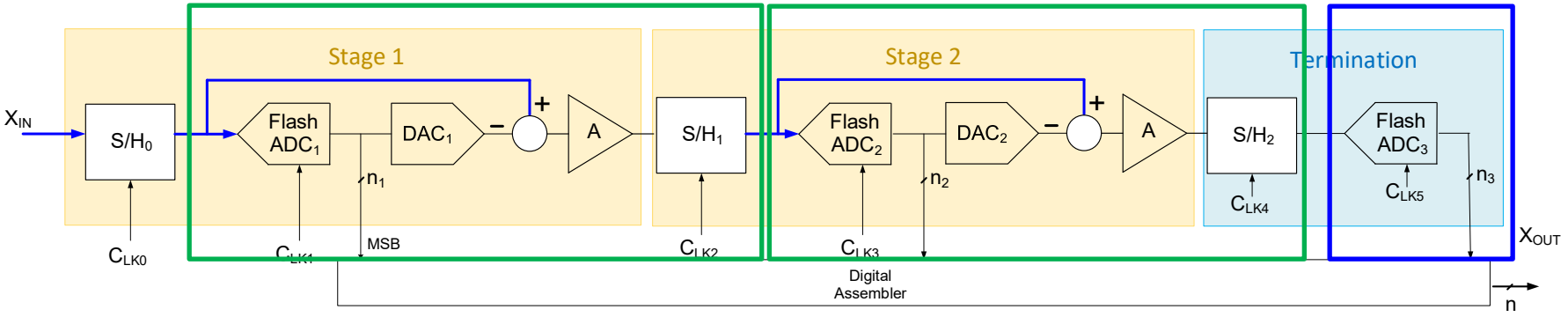
$$N_2 = 2^{n_2}$$

A_1 is typically N_1 A_2 is typically N_1 Often $A_1 =_{A2}$ though not necessarily

- S/H1 frees first stage to take another sample during second stage conversion
- S/H2 frees second stage to take another sample during third stage conversion
- This has a pipelining capability
- The pipelined approach dramatically improves speed (close to Flash if A is fast)
- Significantly reduces the number of comparators
- Introduces latency but not of concern in most applications

– Performance of A amplifiers and S/H can be demanding
– But even more complexity is of concern !!!

Three-Step Flash ADC with Interstage Gain



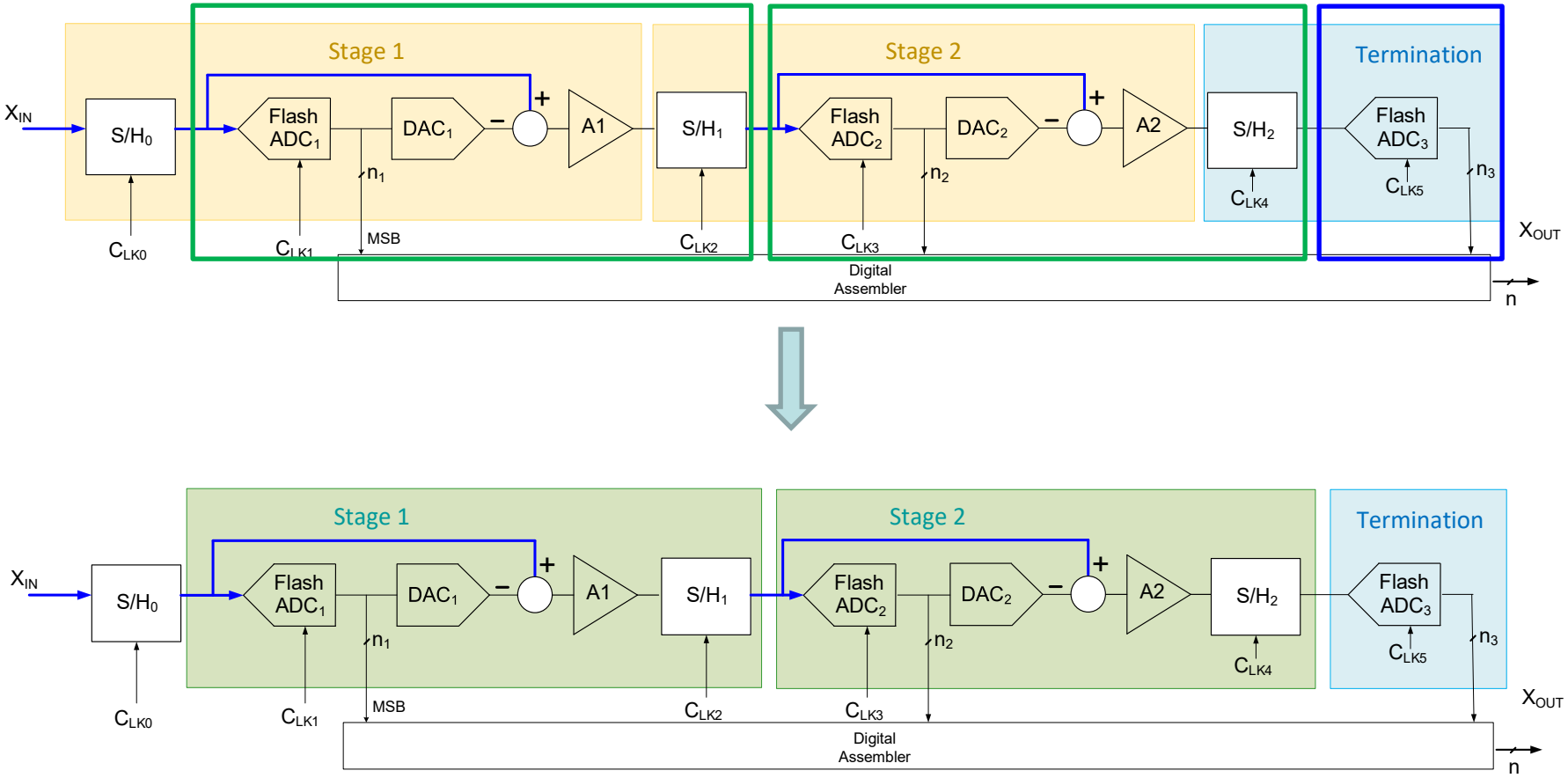
Can be extended to more than 3 stages

- Can go up to 16 bits or maybe a little higher
- Could be as few as one comparator in each Flash ADC
- Further reduction in number of comparators
  (e.g. if one comparator per stage, need only n comparators)
- More latency with more stages but still seldom of concern
- If gains are large enough, comparator offsets in later states can be large
- Will show that with minor modifications, comparator offsets can even be large in first stage

Can partition stages differently

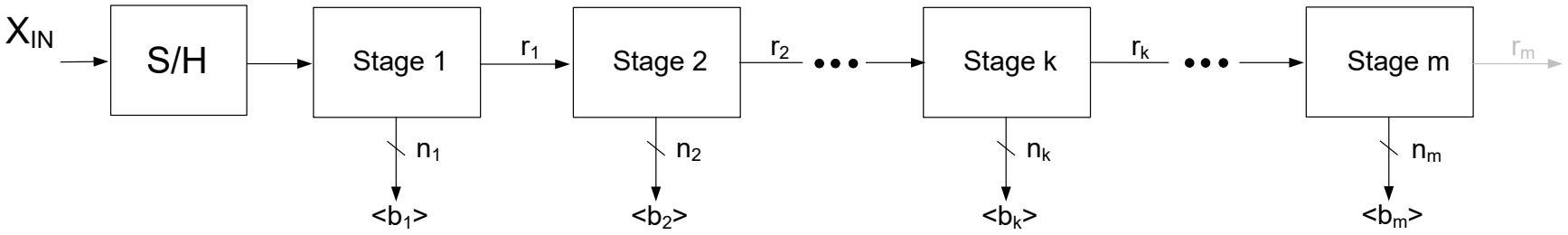
Three-Step Flash ADC with Interstage Gain

Repartitioned Stages



Pipelined ADC

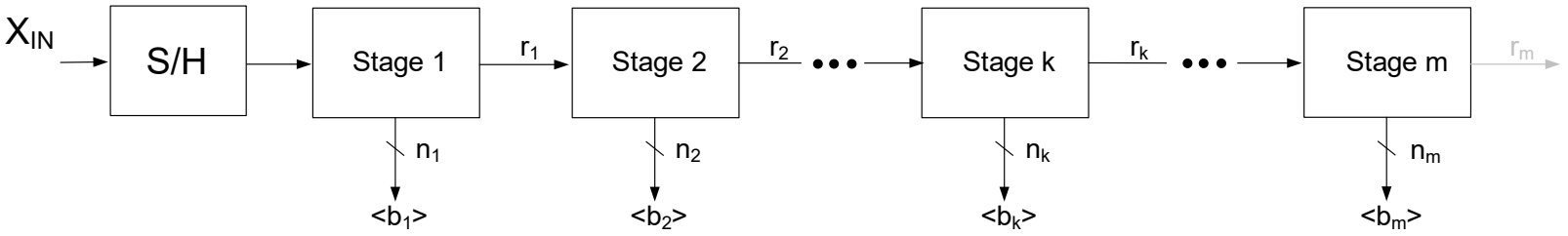
SAR	728
Pipeline	294
Delta Sigma	187
Folding Interpolating	66
Delta Sigma Modulator	9
Two-Step	6
Flash	3
Total	1293



$X_{OUT}=<n_1:n_2:\ldots:n_m>$

- Pipelined structure is widely used
- More than one bit/stage is often used
- Optimal number of bits/stage still an area of debate
- Conceptually can simply design one stage and then copy/paste to increase resolution
- Accuracy (and correspondingly power) in latter stages can be dramatically reduced
- Latency is inherent but not an issue in most applications
- Most power consumed in op amps
- Power dominantly allocated to S/H and MSB stages

Pipelined ADC



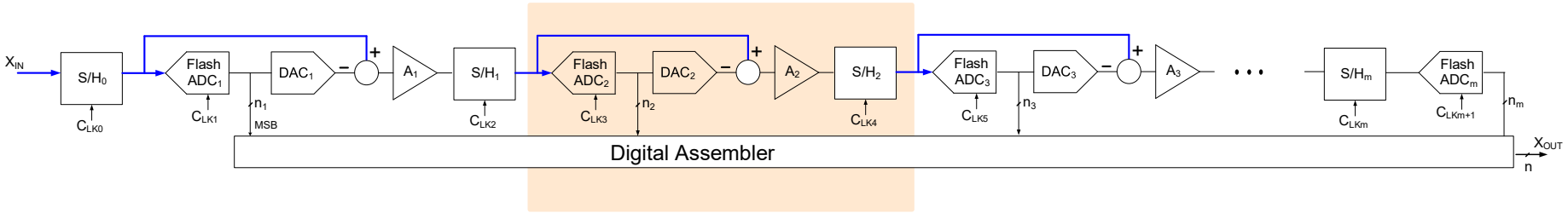
Digital Assembler can simply concatenate individual outputs for some stage architectures

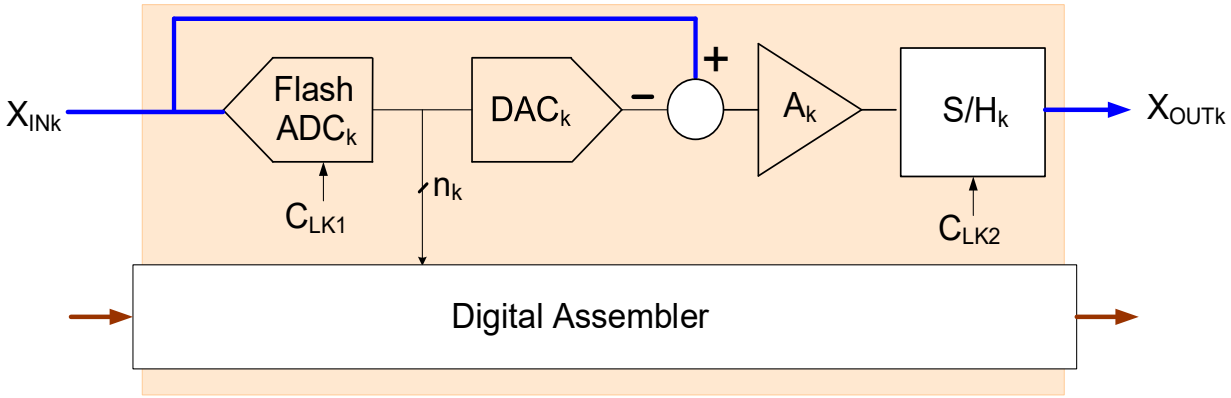
$$X_{OUT}=<n_1:n_2:\ldots:n_m>$$

In this case the Digital Assembler can be a set of m-parallel shift-register blocks with output on the last stage

Latency is equal to the number of stages times the conversion time/stage

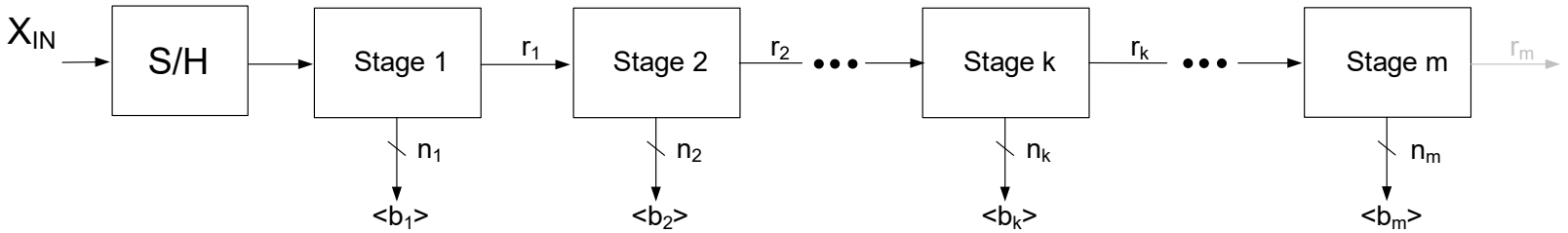
Pipelined ADC

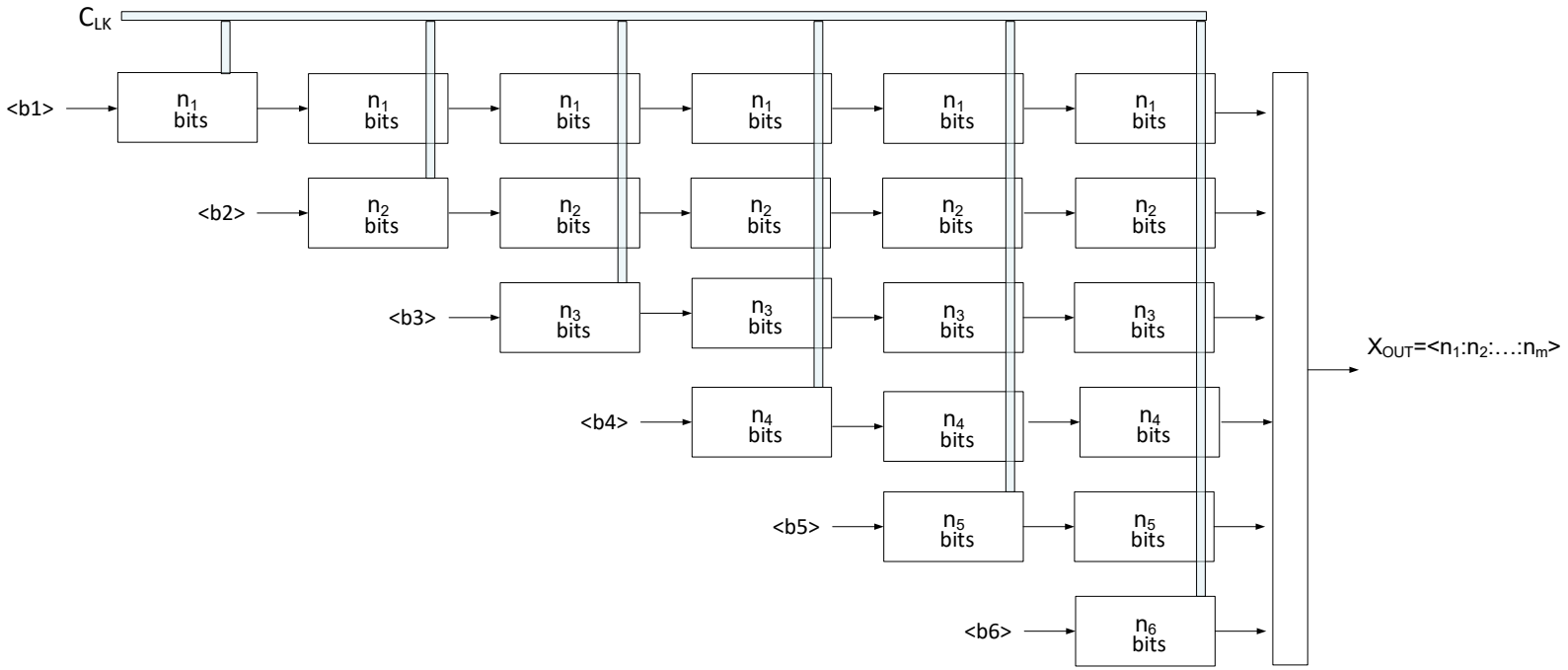




Pipeline Stage

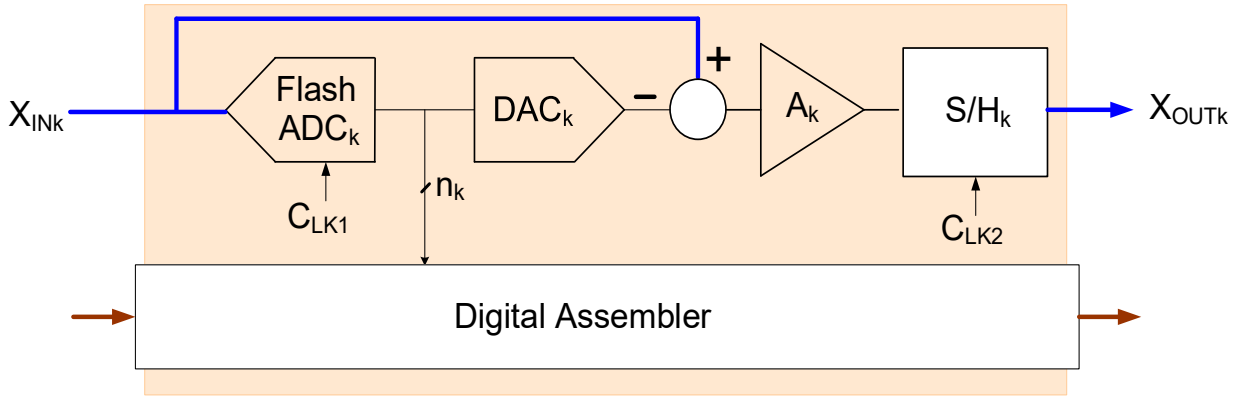
Pipelined ADC





Digital Assembler

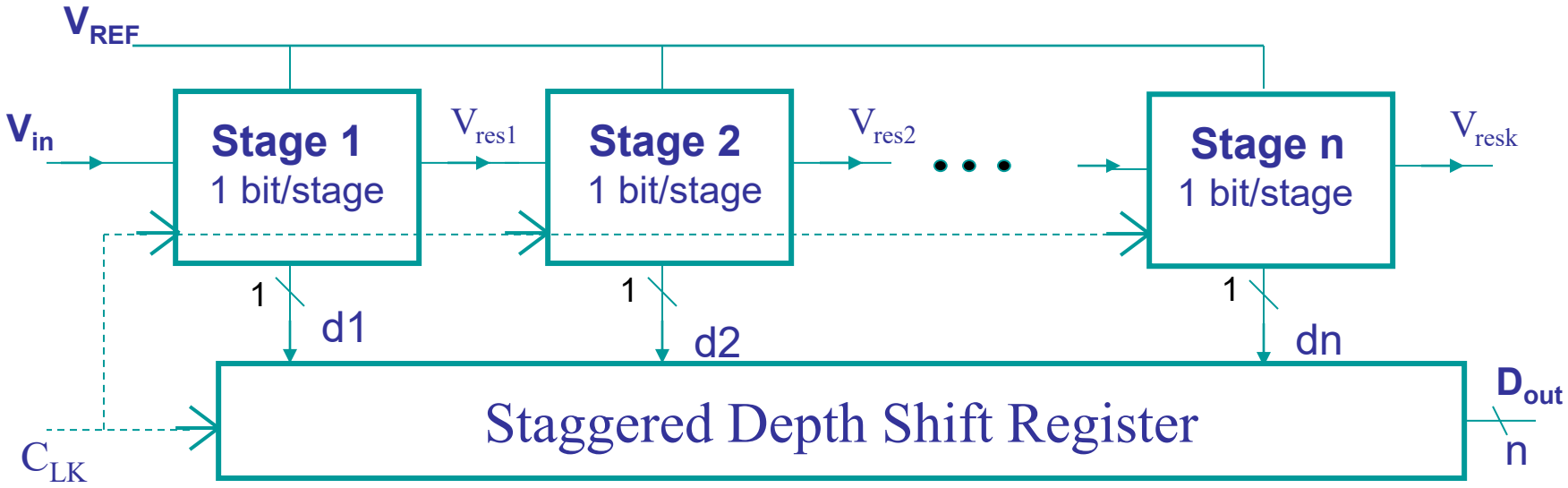
Pipeline Stage



- Appears to be lots of complexity
- S/H is sampling a near-static signal on all stages (except stage 0)
- Ideally the stage gain is chosen to achieve maximum signal level at the output if V_{REF} fixed for each stage
- Will show that dominant source of power dissipation is typically the amplifier

Example of 1 bit/stage pipeline

- A=2
- ADC is simply comparator in each stage
- Stages could be identical though often relaxed requirements on latter stages to reduce power



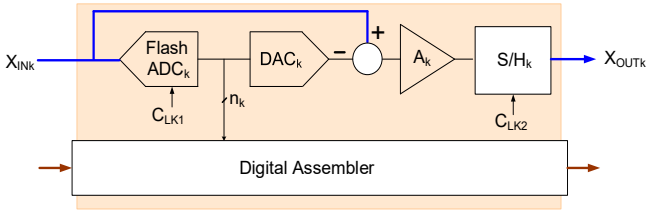
D_{OUT} = <d1 d2 … dn>

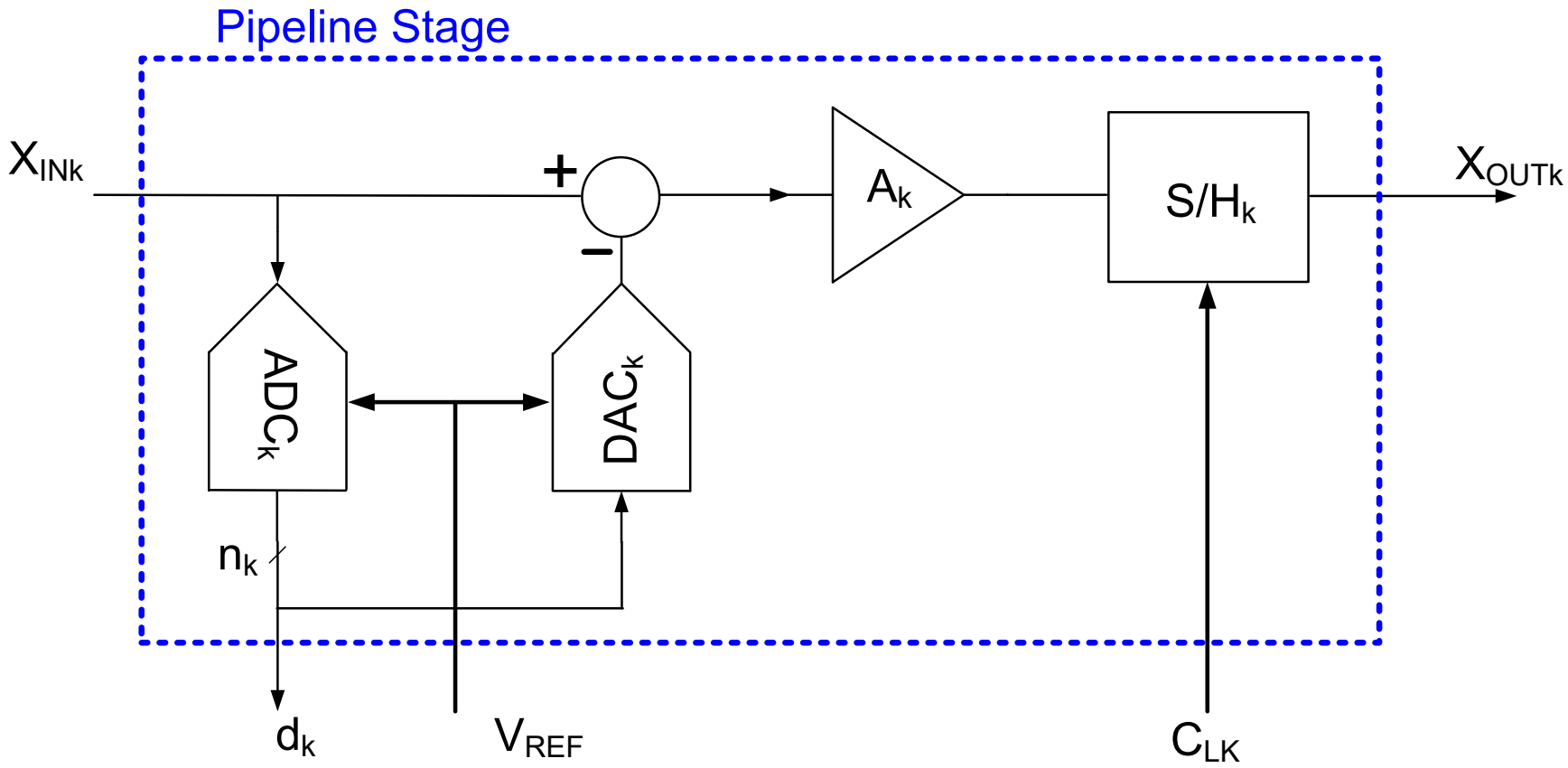
$$V_{OUT} = V_{REF} \sum_{i=1}^{n} \frac{d_i}{2^i}$$

- Functional form of output particularly attractive and simple
- Similar relationship for any integral number of bits/stage

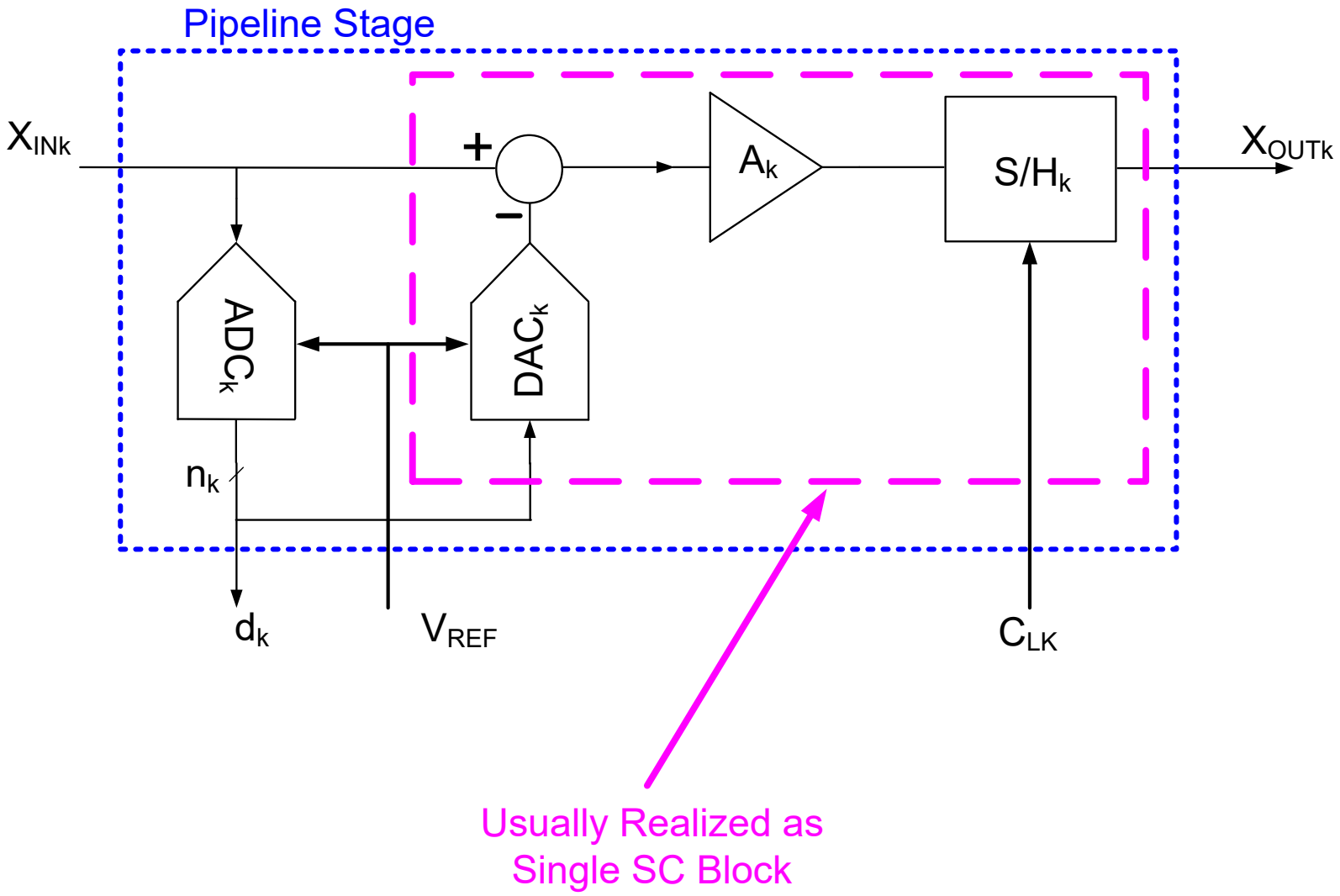
Pipelined ADC Stage k

(Redrawn for convenience)

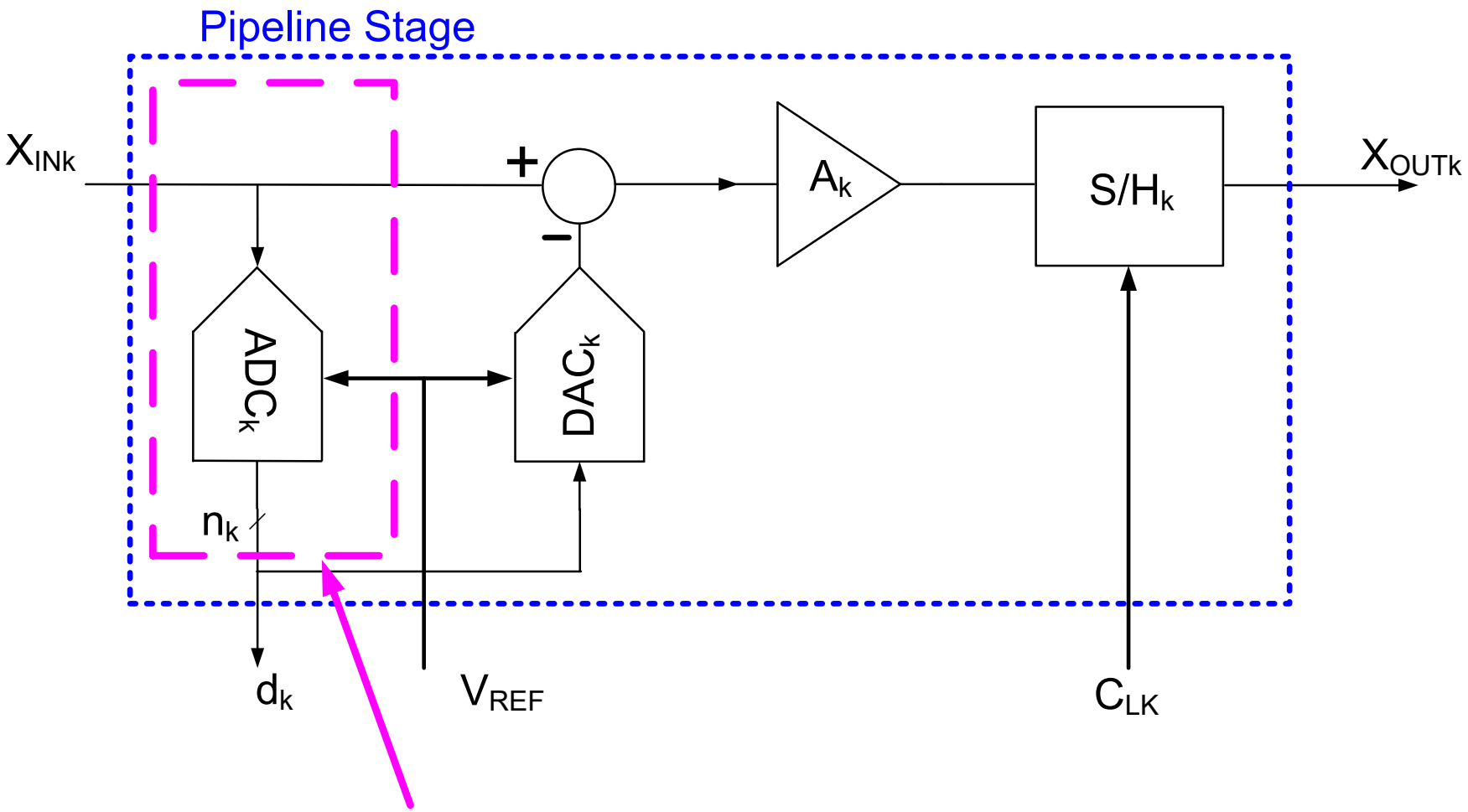




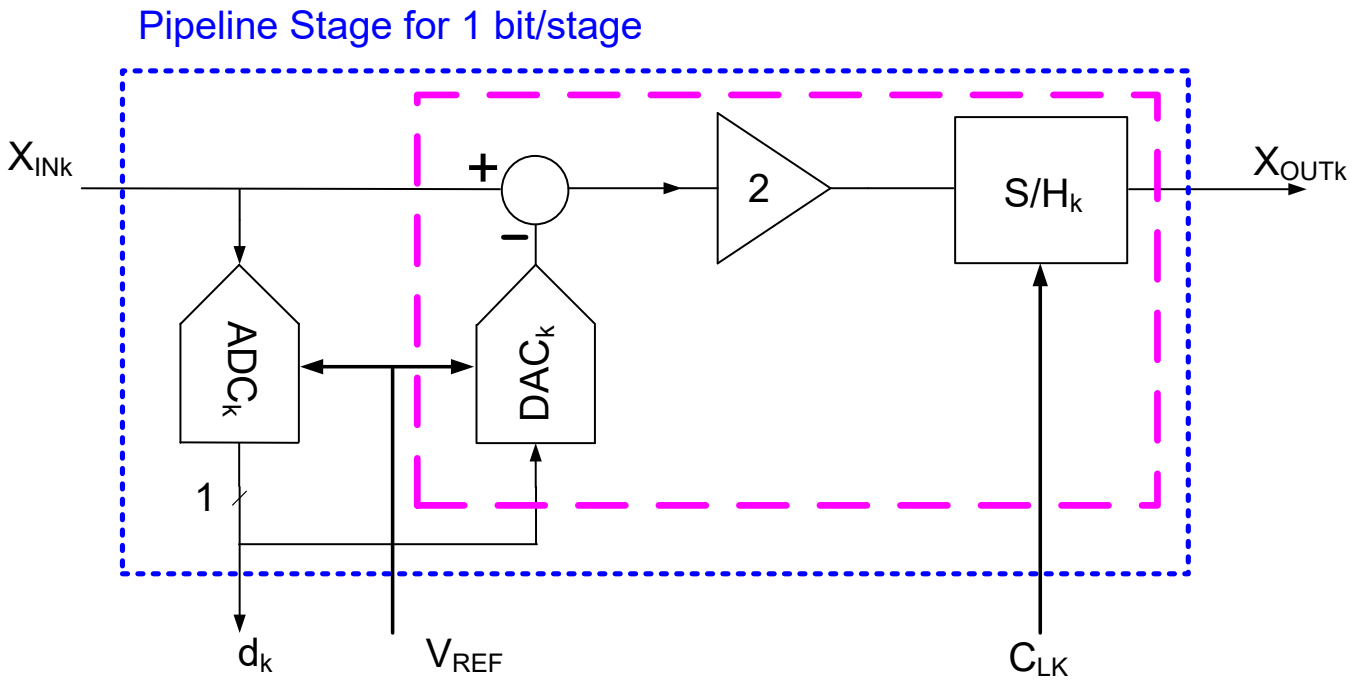
Pipelined ADC Stage k



Pipelined ADC Stage k



Pipelined ADC Stage k

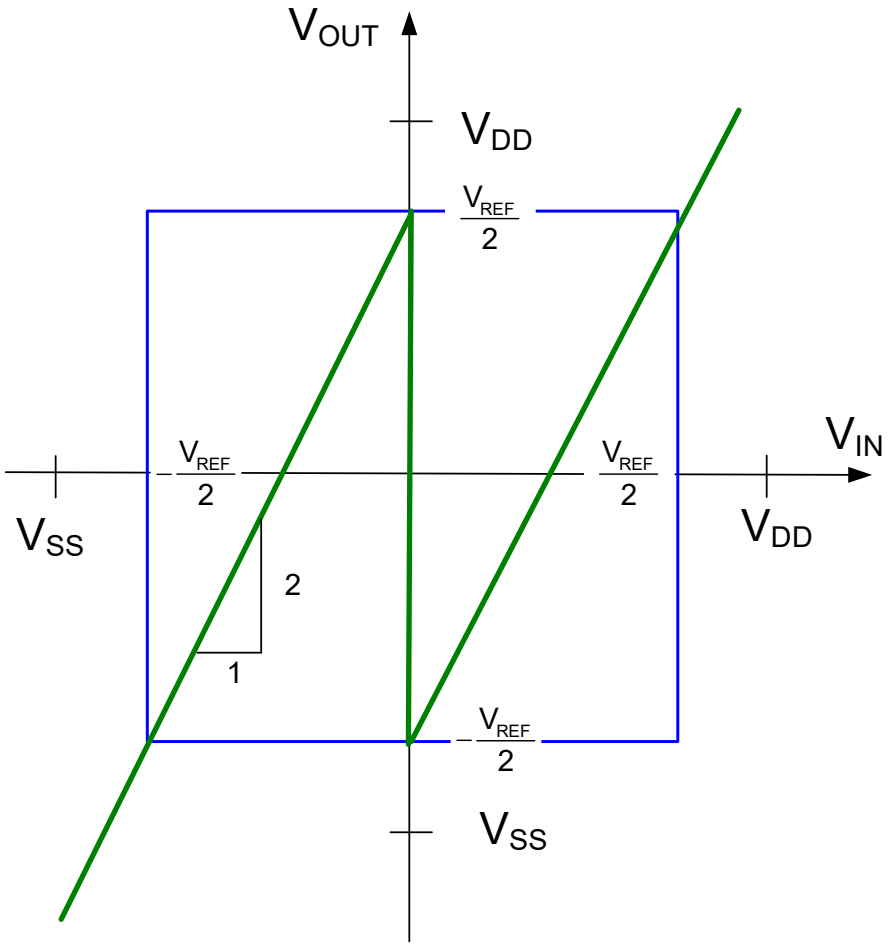


Assuming $-\frac{V_{REF}}{2} < V_{IN} < \frac{V_{REF}}{2}$

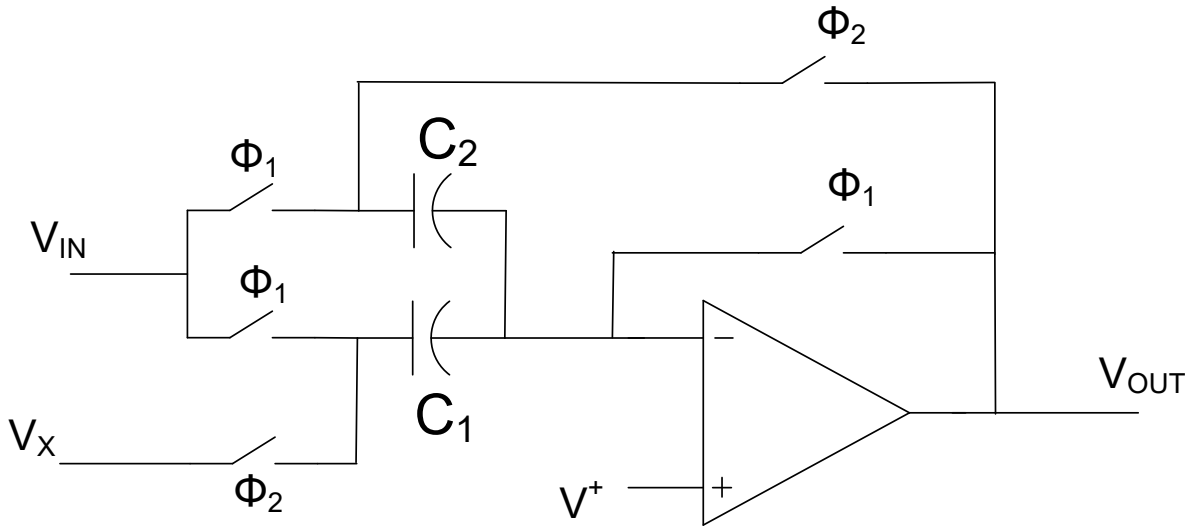
$$V_O = \begin{cases} 2V_{IN} + \frac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \frac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

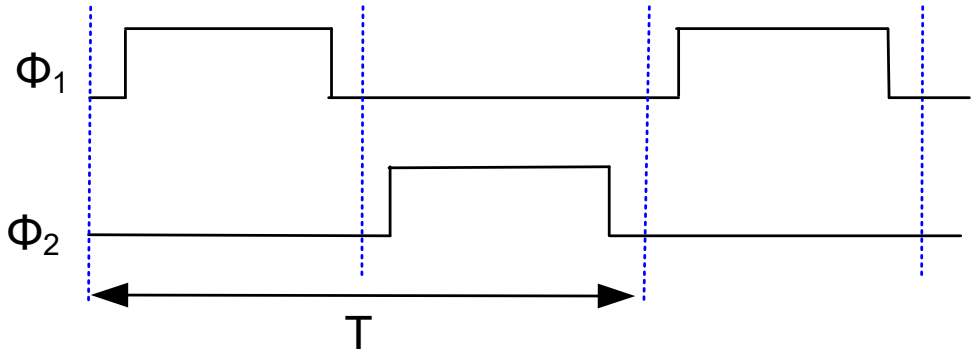
Ideal Transfer Characteristics for 1 bit/stage

$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$



Consider the following circuit





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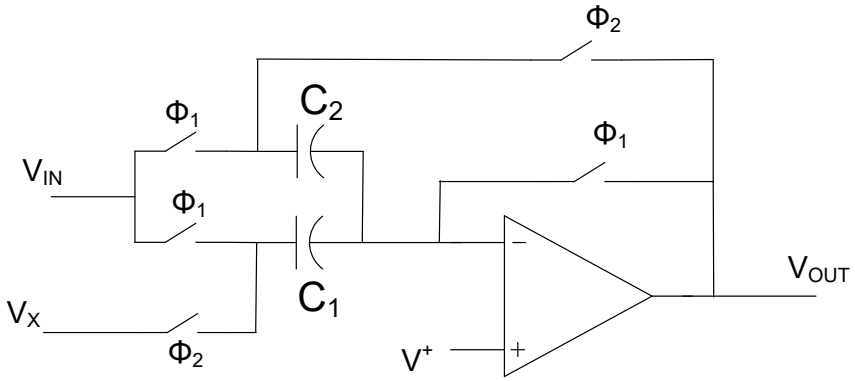
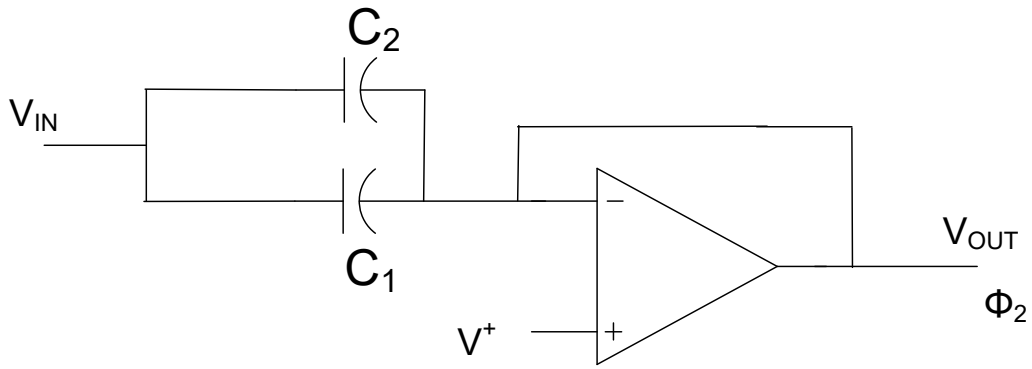


During Φ_1



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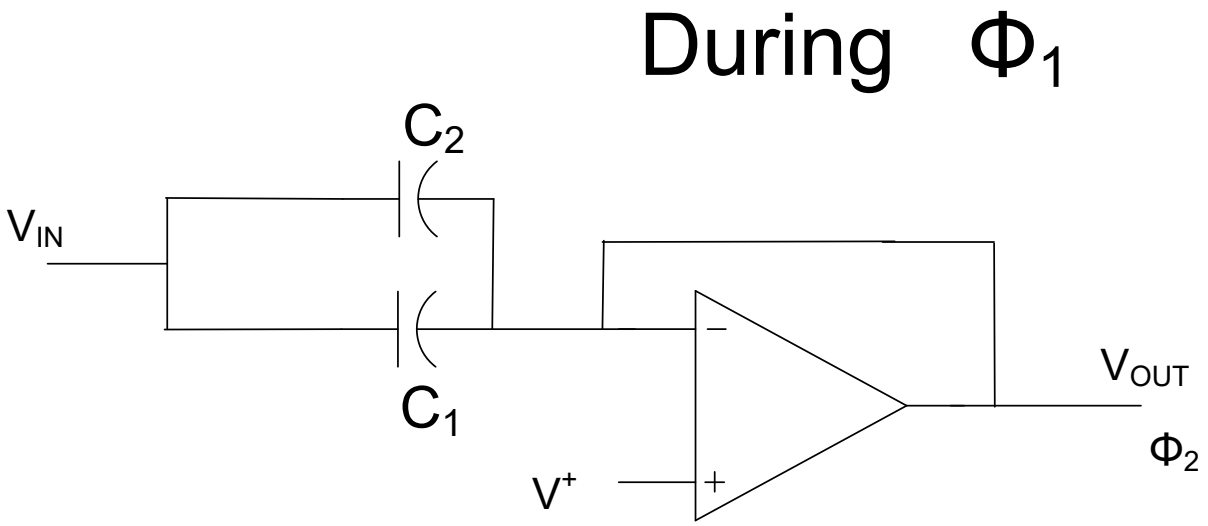
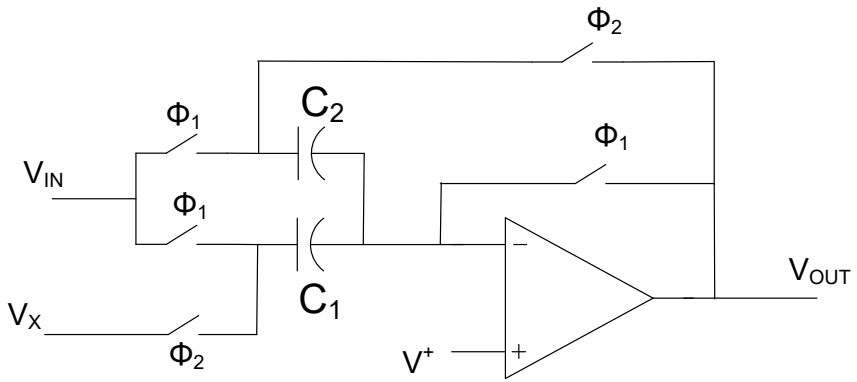
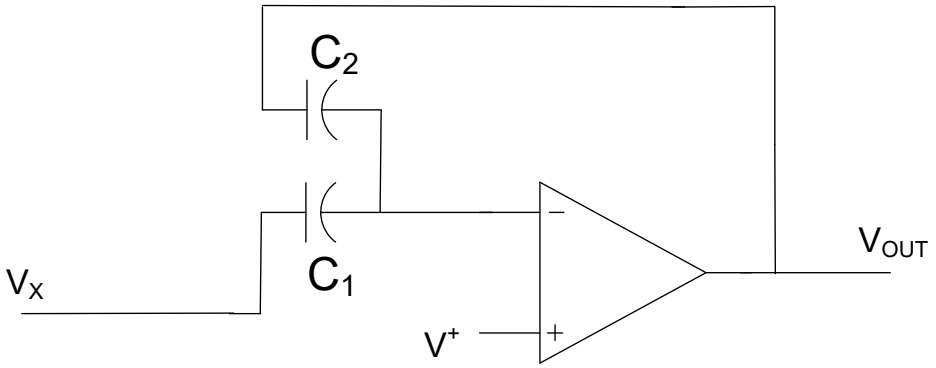


$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

Consider the following circuit



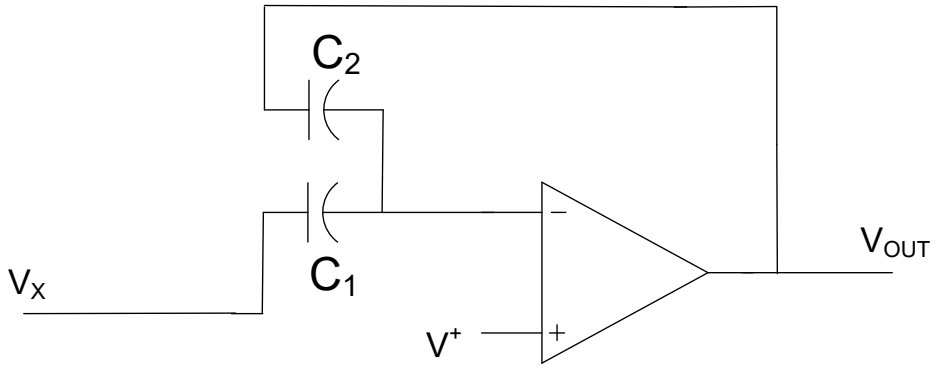
During Φ_2



Consider the following circuit

$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

During Φ_2



Define Q_{1T} to be the charge transferred from C_1 during phase Φ_2

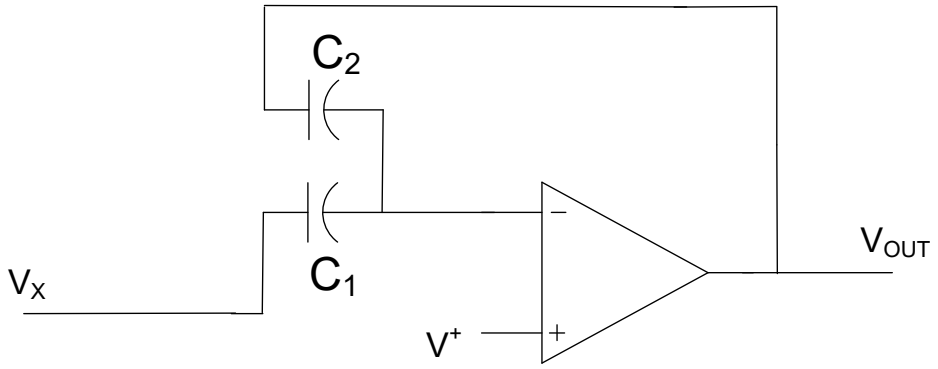
$$Q_{1T} = C_1\left(V_{IN} - V^+\right) - C_1\left(V_X - V^+\right) = C_1\left(V_{IN} - V_X\right)$$

Define Q_{2F} to be the total charge on C_2 during phase Φ_2

$$Q_{2F} = Q_2 + Q_{1T} = C_2\left(V_{IN} - V^+\right) + C_1\left(V_{IN} - V_X\right) = \left(C_1 + C_2\right)V_{IN} - C_2V^+ - C_1V_X$$

Consider the following circuit

During Φ_2

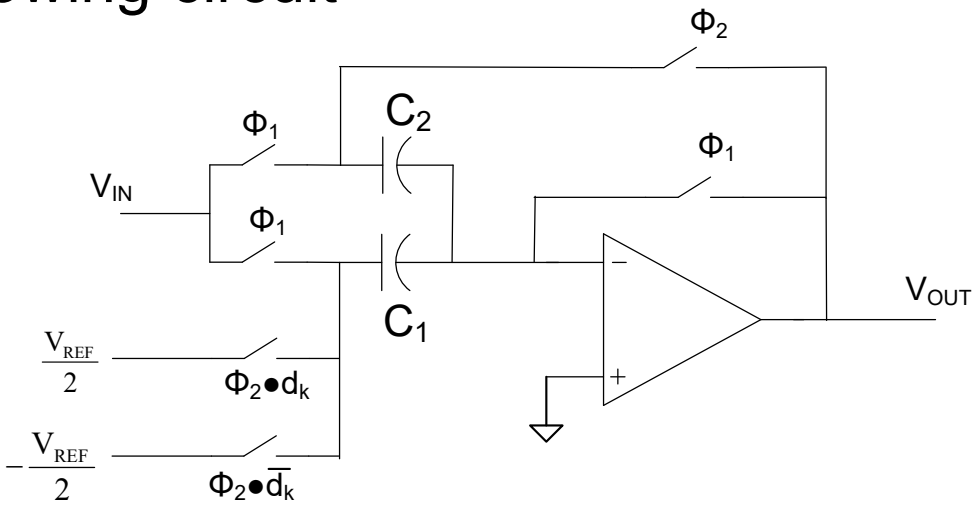


$$Q_{2F} = (C_1 + C_2)V_{IN} - C_2V^+ - C_1V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - V^+ - \frac{C_1}{C_2}V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X$$

Consider the following circuit



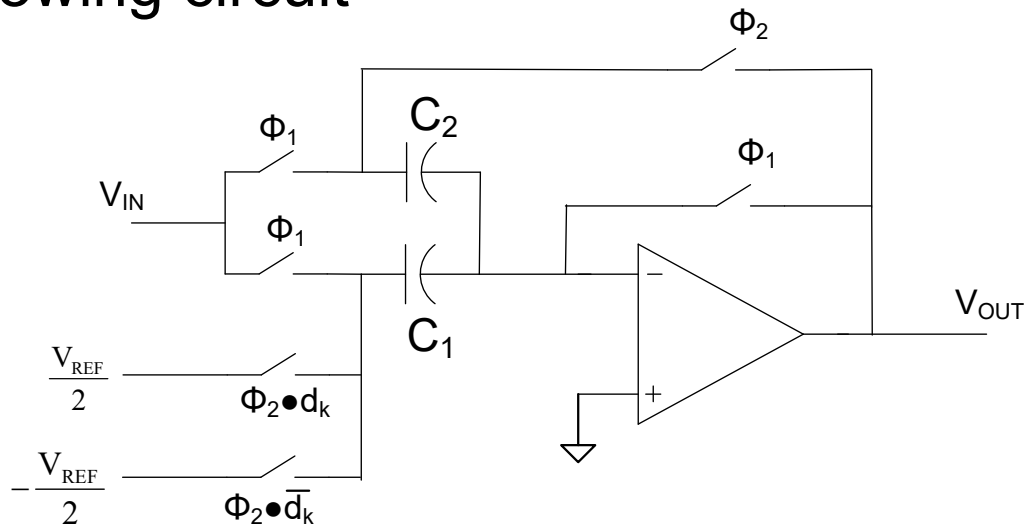
$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

Assume $$V_X = \begin{cases} \frac{V_{REF}}{2} & \text{for } V_{IN} > 0 \\ -\frac{V_{REF}}{2} & \text{for } V_{IN} < 0 \end{cases}$$

If $C_1 = C_2 = C$ and $V_X = -\frac{V_{REF}}{2}$ i.e. $V_{IN} < 0$

$$V_{OUTF} = 2V_{IN} + \frac{V_{REF}}{2}$$

Consider the following circuit



$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

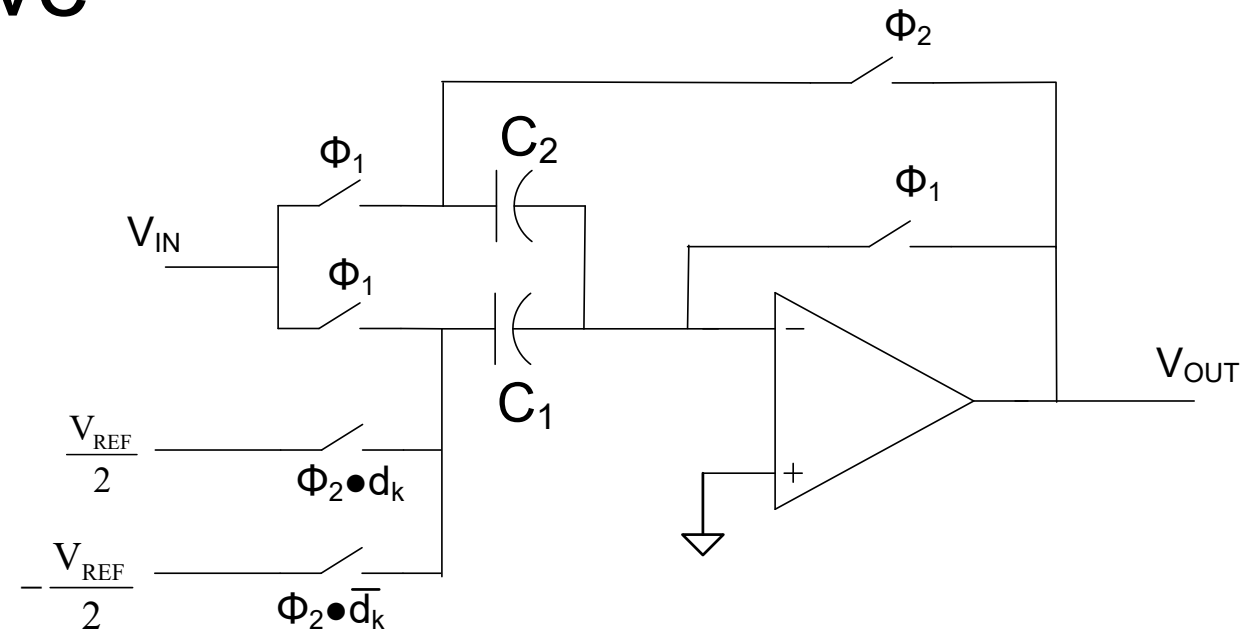
$$V_X = \begin{cases} \frac{V_{REF}}{2} & \text{for } V_{IN} > 0 \\ -\frac{V_{REF}}{2} & \text{for } V_{IN} < 0 \end{cases}$$

Likewise

If $C_1 = C_2 = C$ and $V_X = \frac{V_{REF}}{2}$ i.e. $V_{IN} > 0$

$$V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2}$$

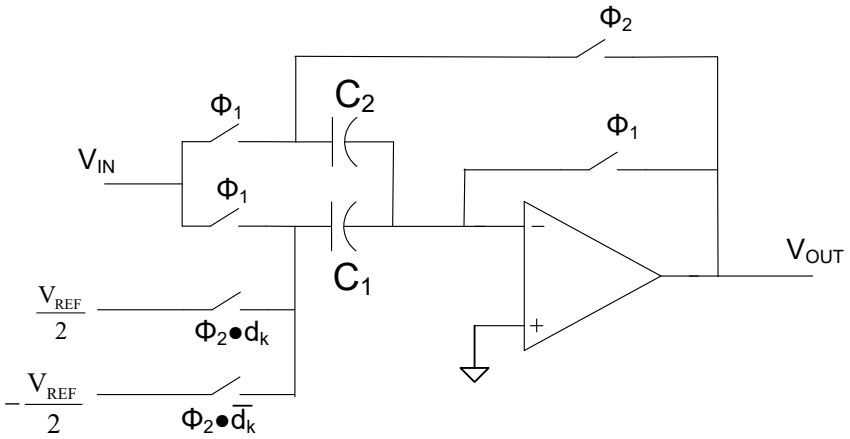
Observe

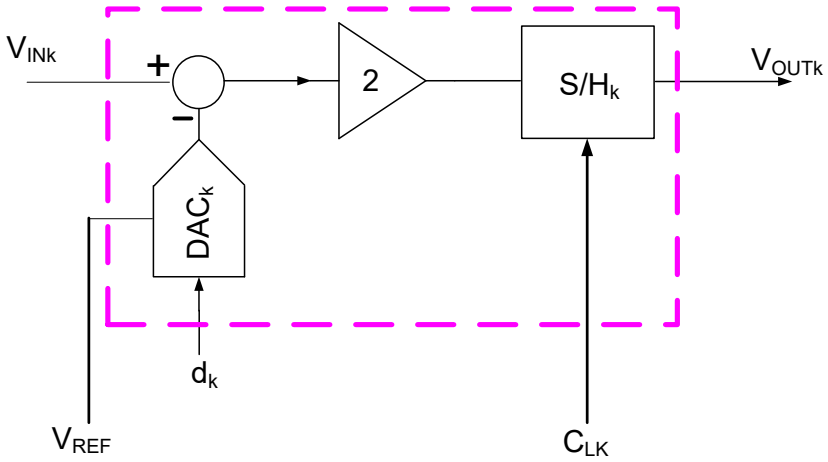


Thus, summarizing

$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

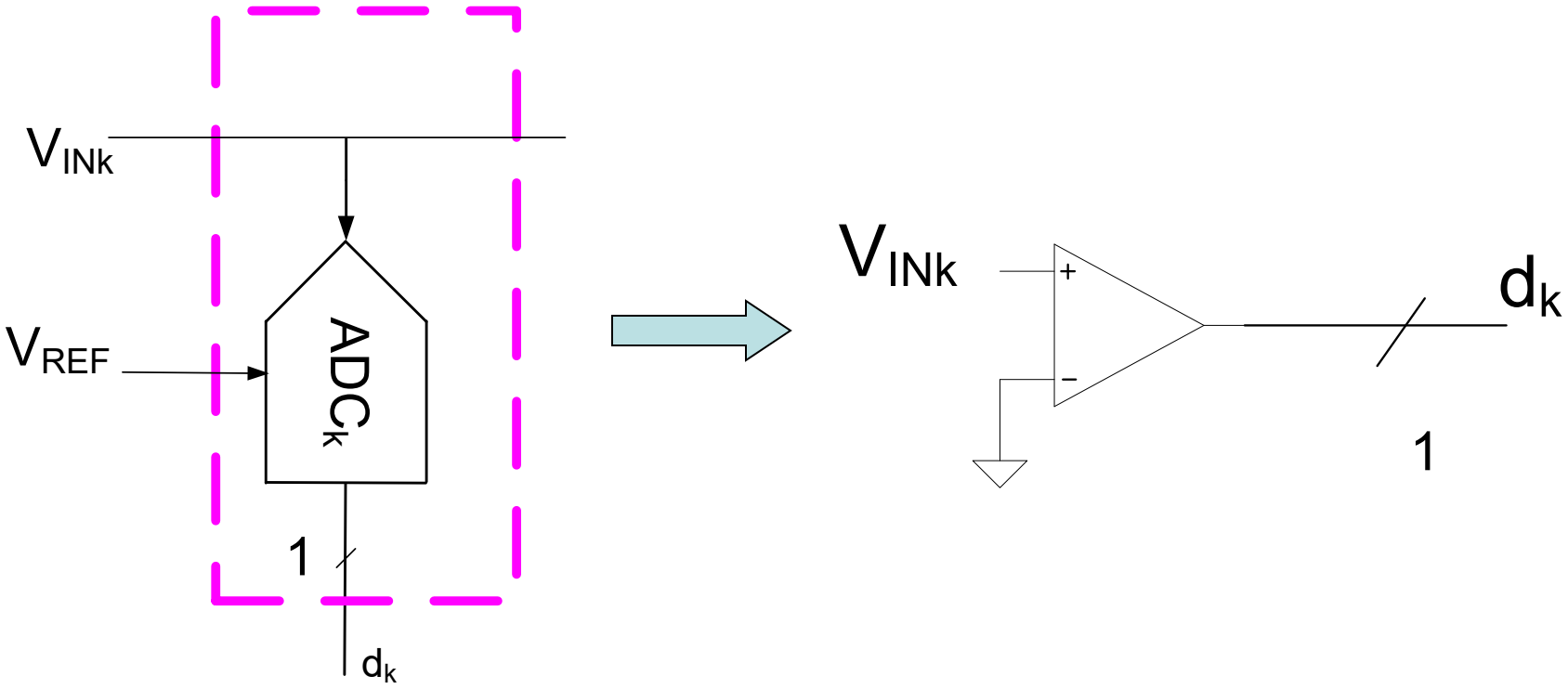
1-bit/Stage Pipeline Implementation



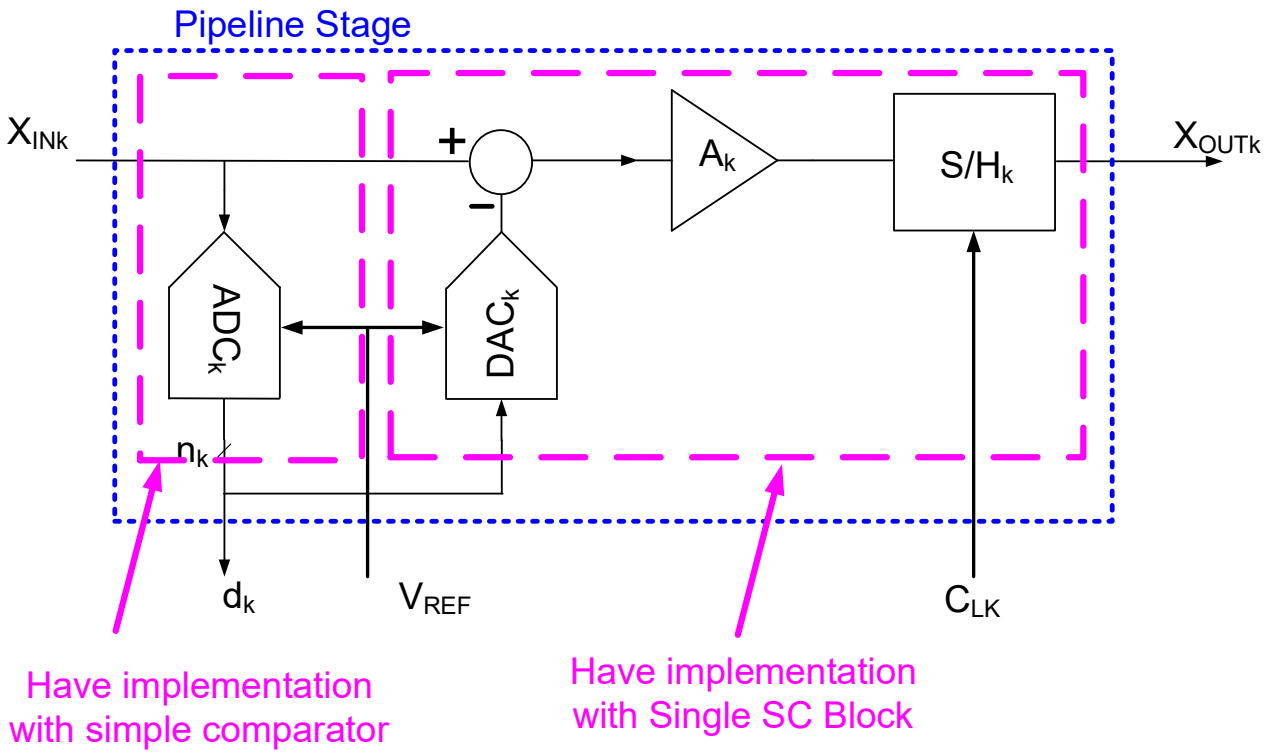


$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

1-bit/Stage Pipeline Implementation

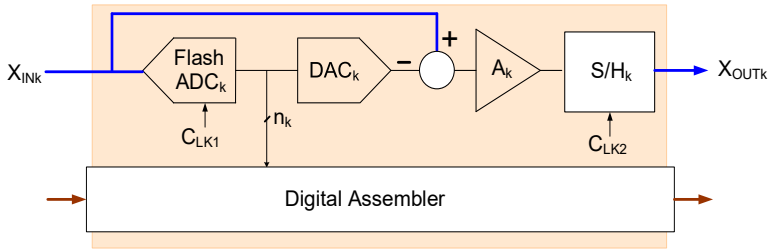


Pipelined ADC Stage k



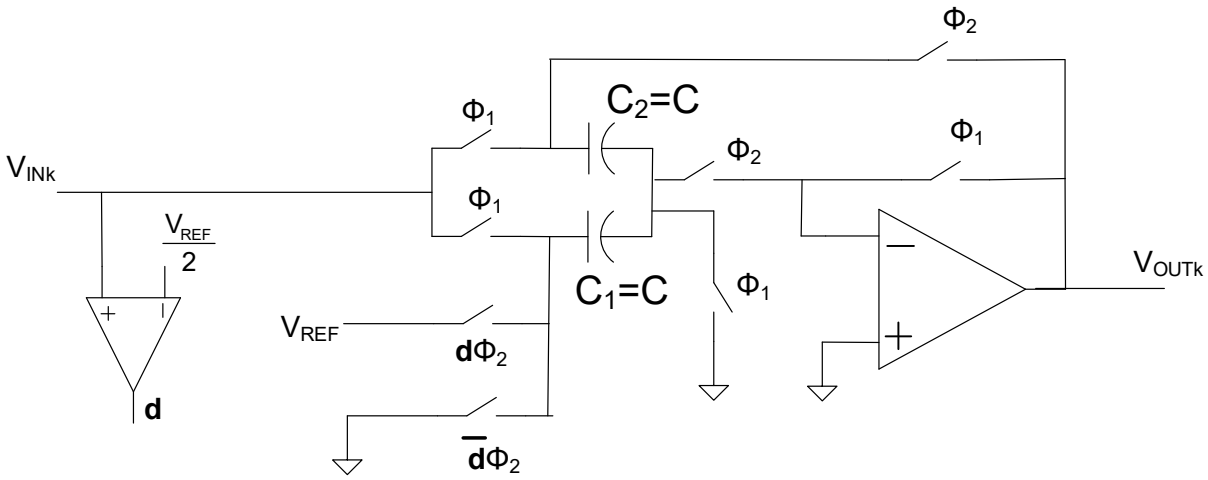
- Have shown simple implementation with 1-bit/stage structure
- Implementations with 2-bits/stage or 3-bits/stage also straightforward

Typical SC Pipeline Stage

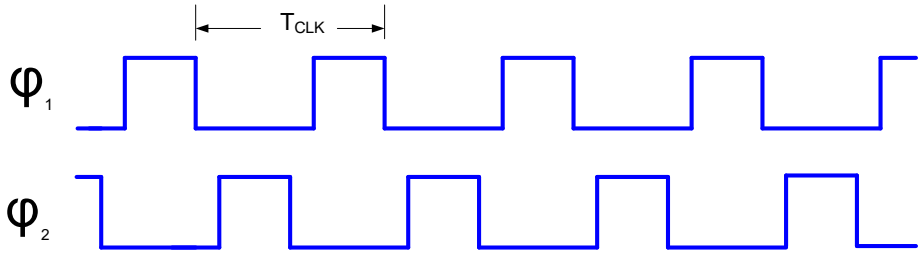


Very simple and compact stages are used

For 1 bit/stage (Digital Assembler not shown)

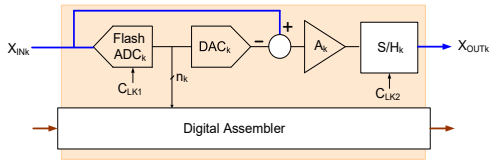


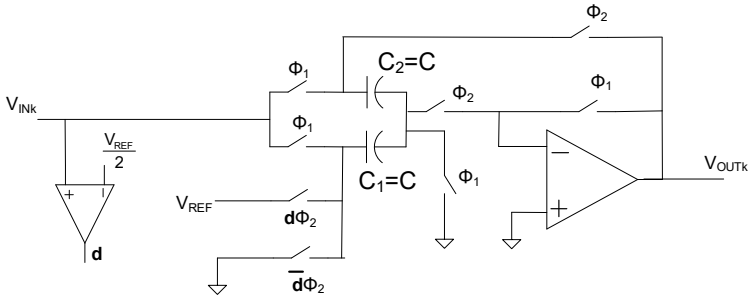
Clock is complimentary nonoverlapping

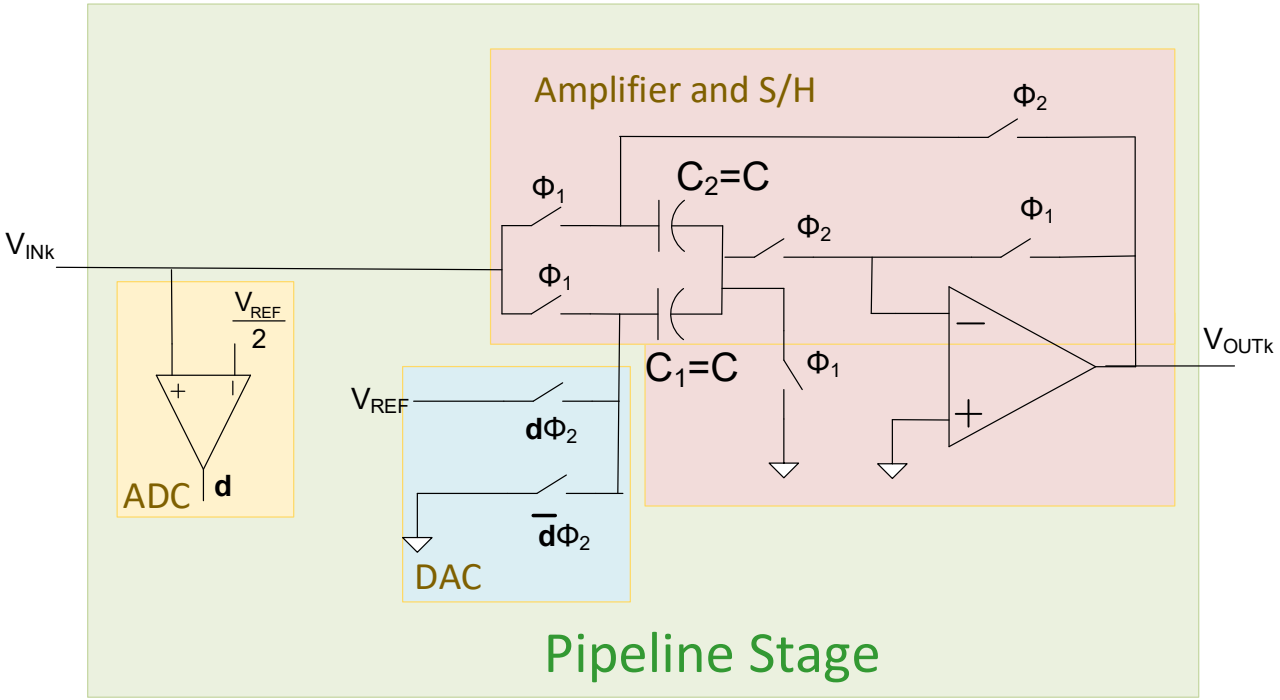


Typical SC Pipeline Stage

For 1 bit/stage (Digital Assembler not shown)

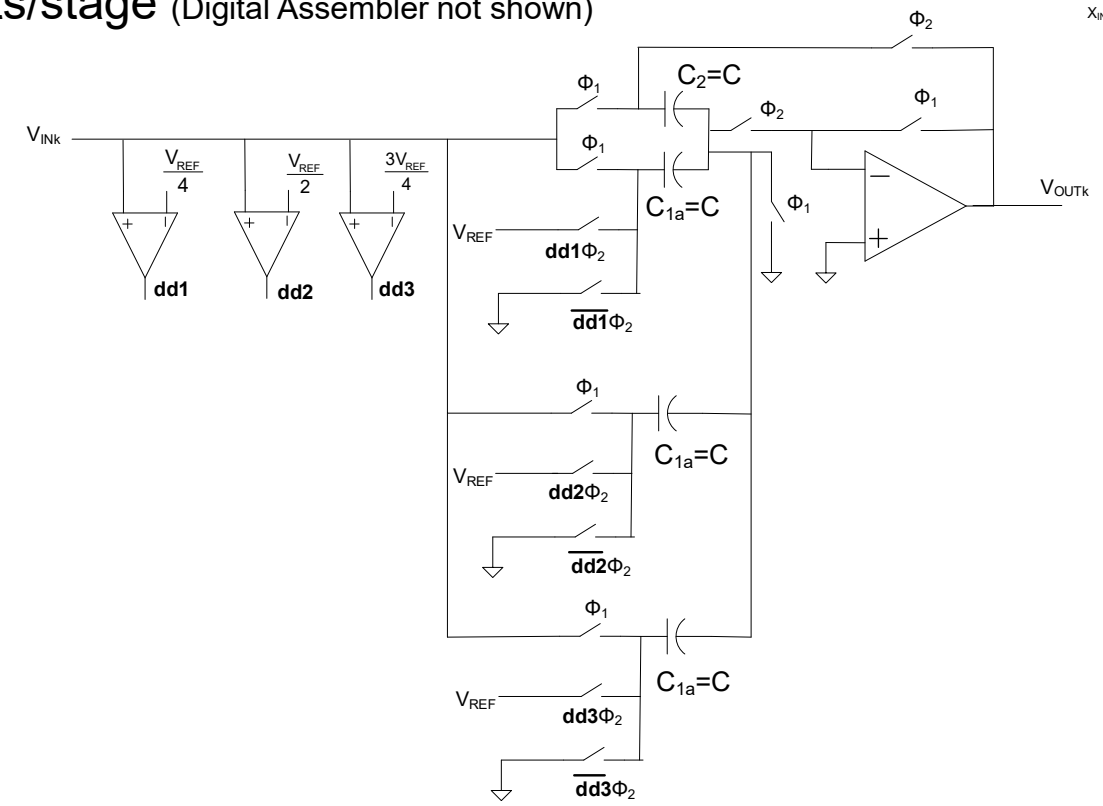


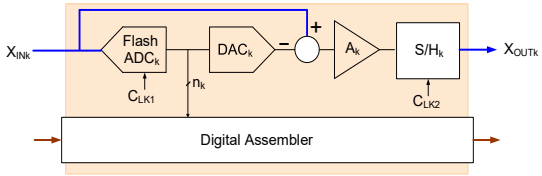




Typical SC Pipeline Stage

For 2 bits/stage (Digital Assembler not shown)





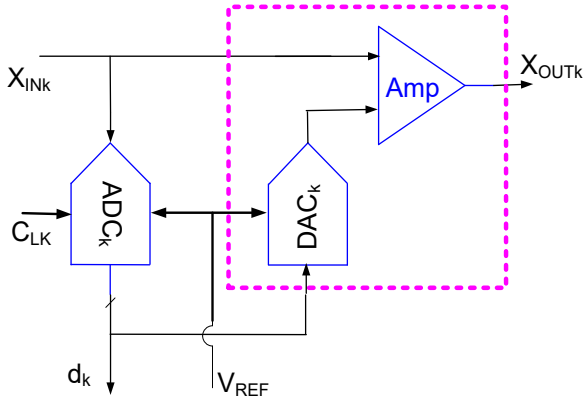
Gain =4

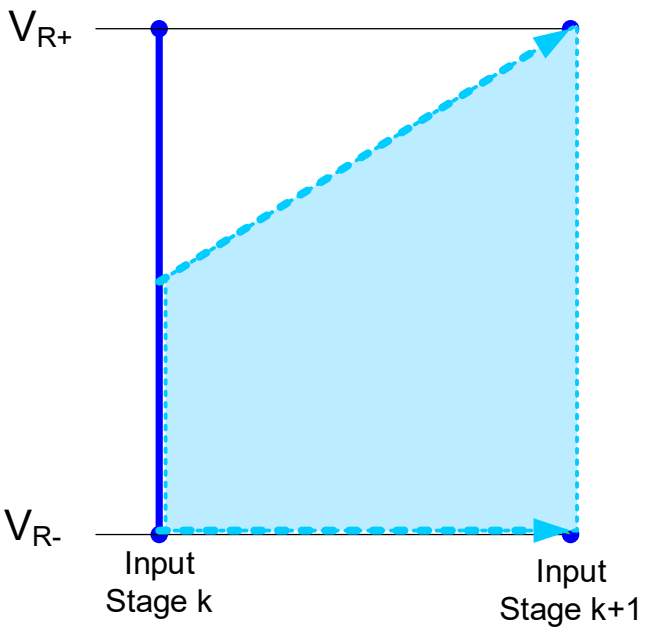
$$V_{OUT}=V_{IN}\left(1+\frac{C_{1a}+C_{1b}+C_{1c}}{C_2}\right)-\left(d_{d1}\left(\frac{C_{1a}}{C_2}\right)+d_{d2}\left(\frac{C_{1b}}{C_2}\right)+d_{d3}\left(\frac{C_{1c}}{C_2}\right)\right)V_{REF} \Rightarrow V_{OUTk}=4V_{INk}-\left(d_{dd1}+d_{dd2}+d_{dd3}\right)V_{REF}$$

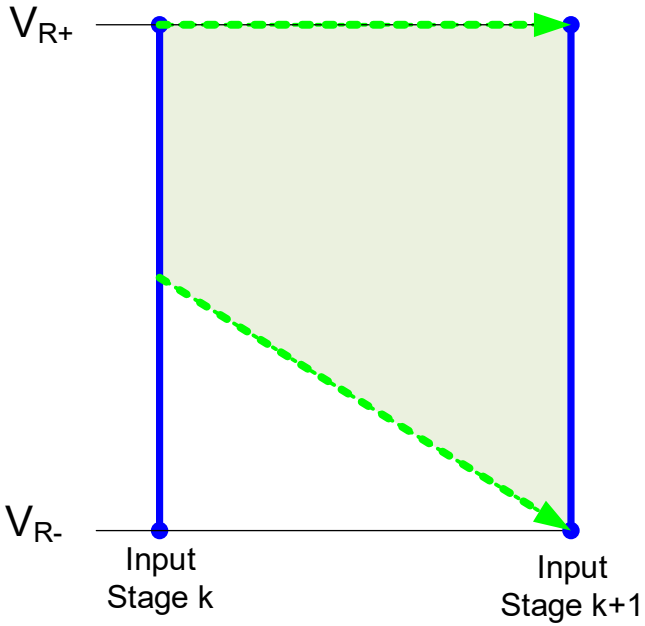
- Directly use thermometer code outputs
- Can be extended to more bits/stage
- Accurate gain possible with good layout

Operation of Pipelined Amplifier

Ideal transfer characteristics (1 bit/stage)

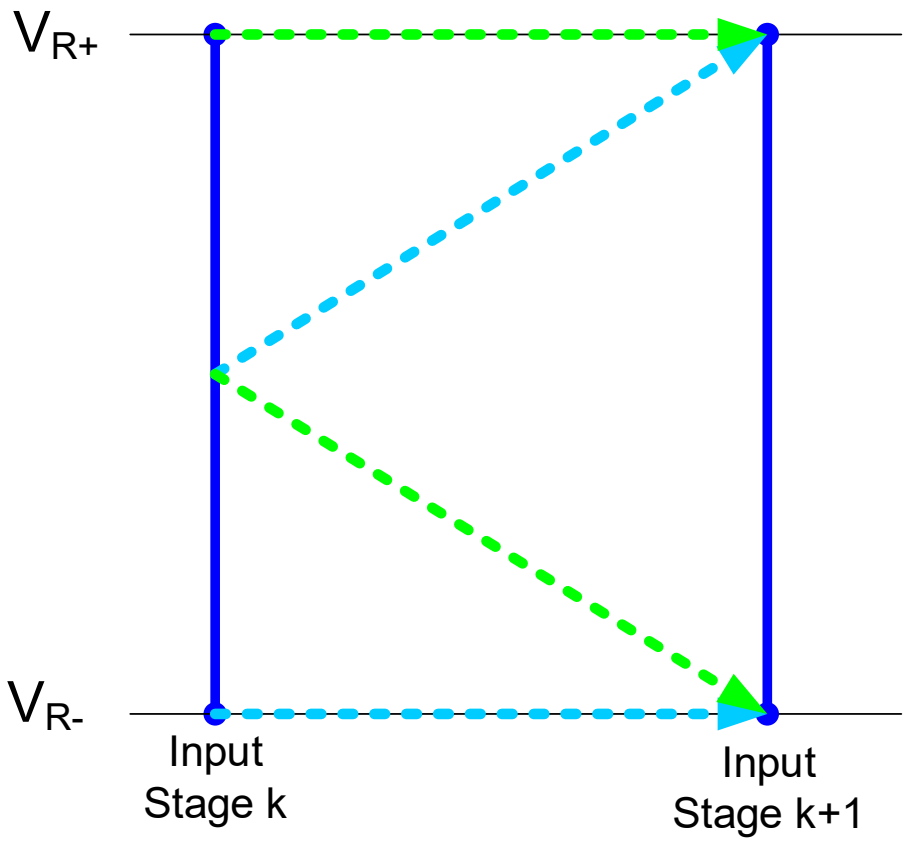


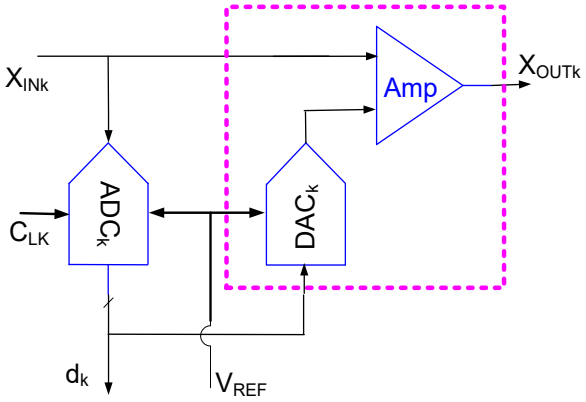




Operation of Pipelined Amplifier

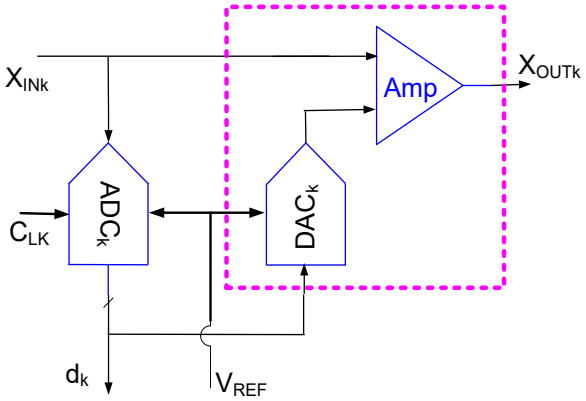
Ideal transfer characteristics (1 bit/stage)

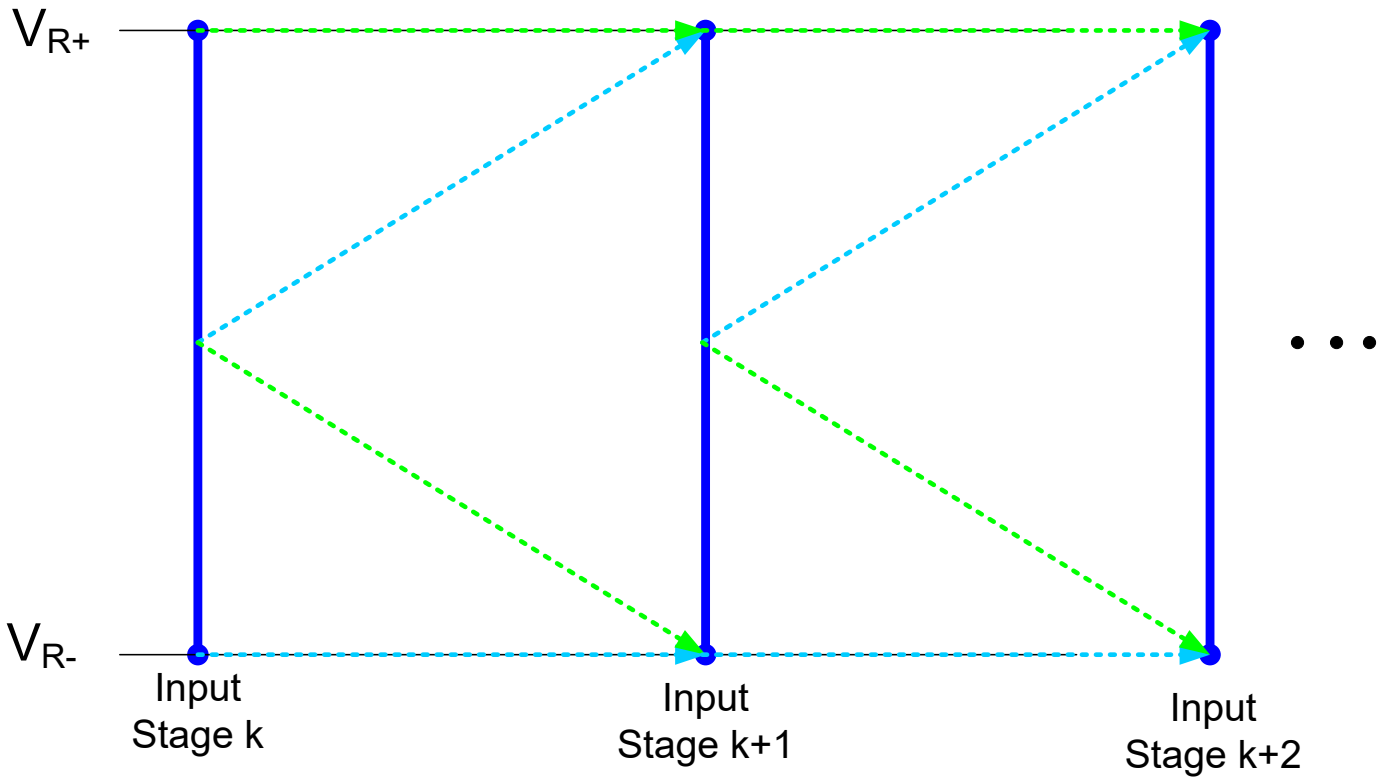




Operation of Pipelined Amplifier

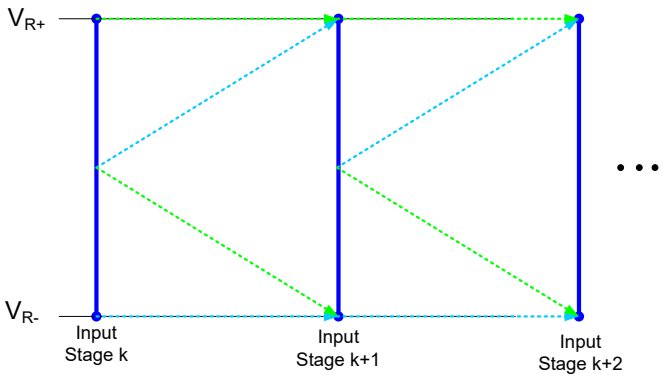
Ideal transfer characteristics (1 bit/stage)

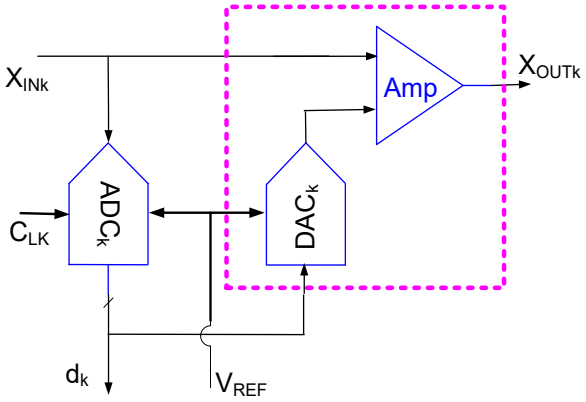


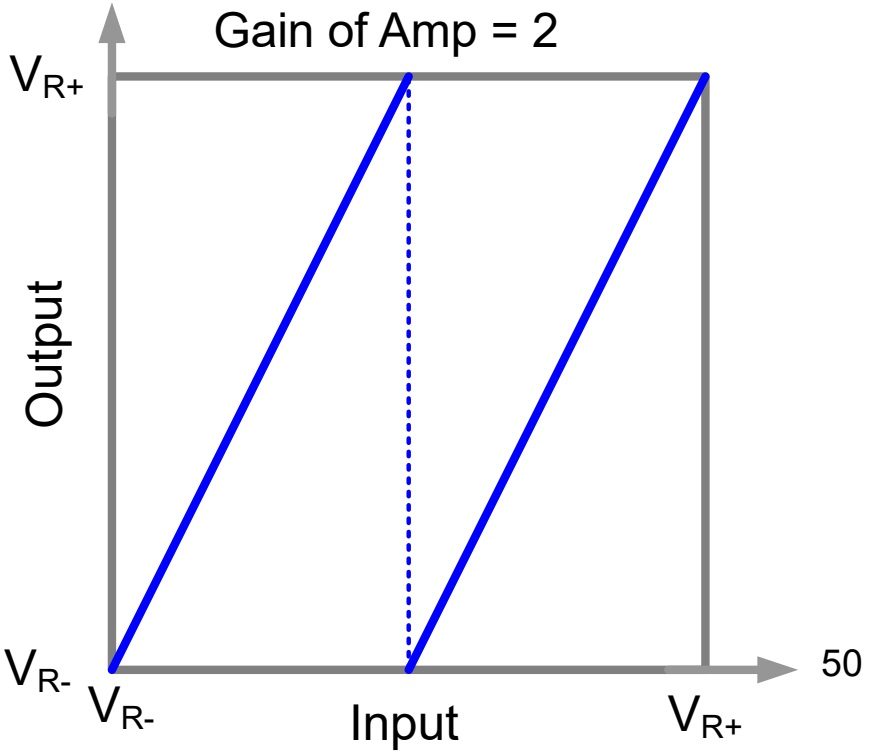


Operation of Pipelined Amplifier

Ideal transfer characteristics (1 bit/stage)

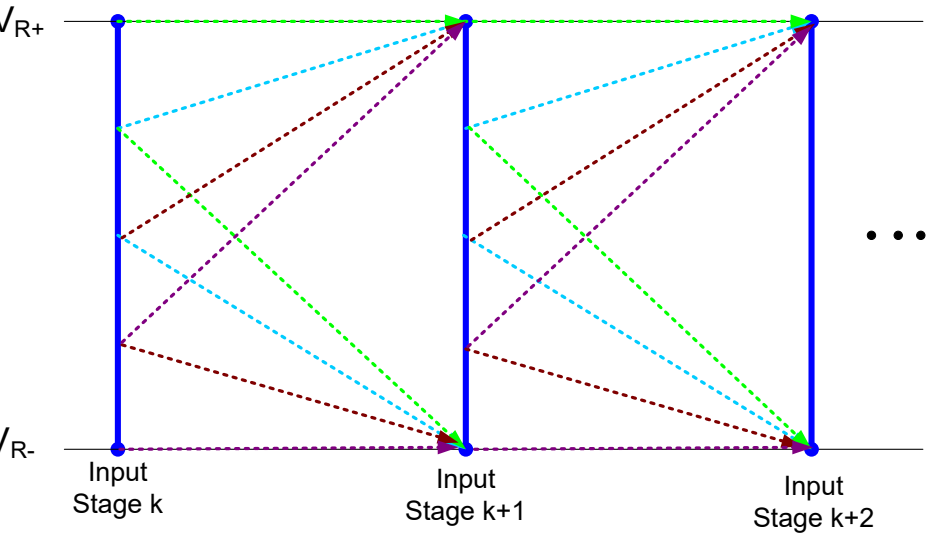


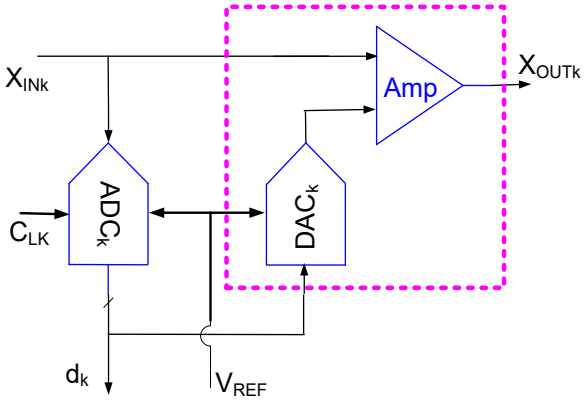


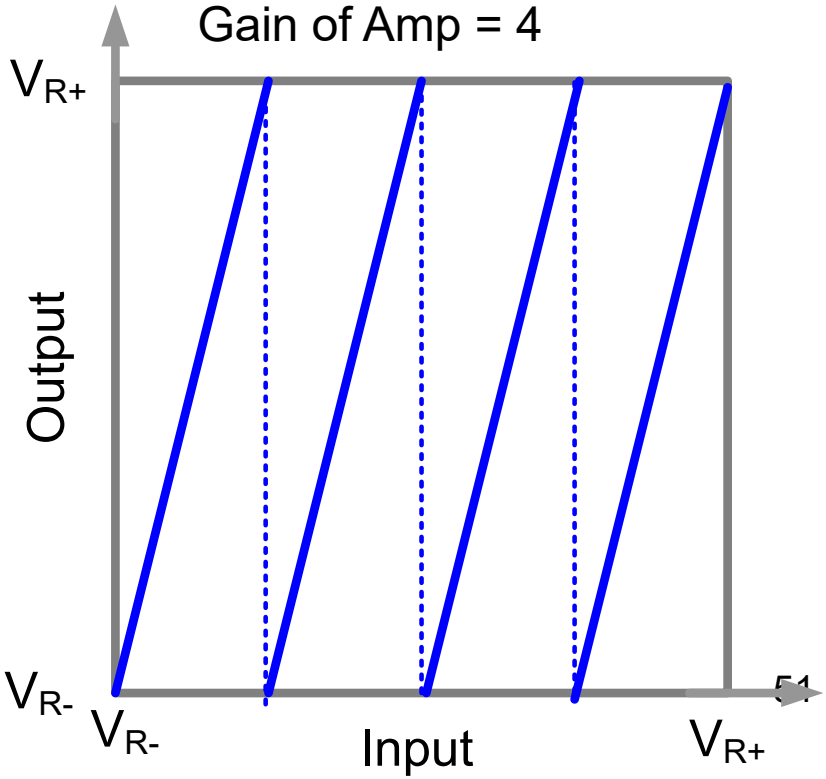


Operation of Pipelined Amplifier

Ideal transfer characteristics (2 bits/stage)

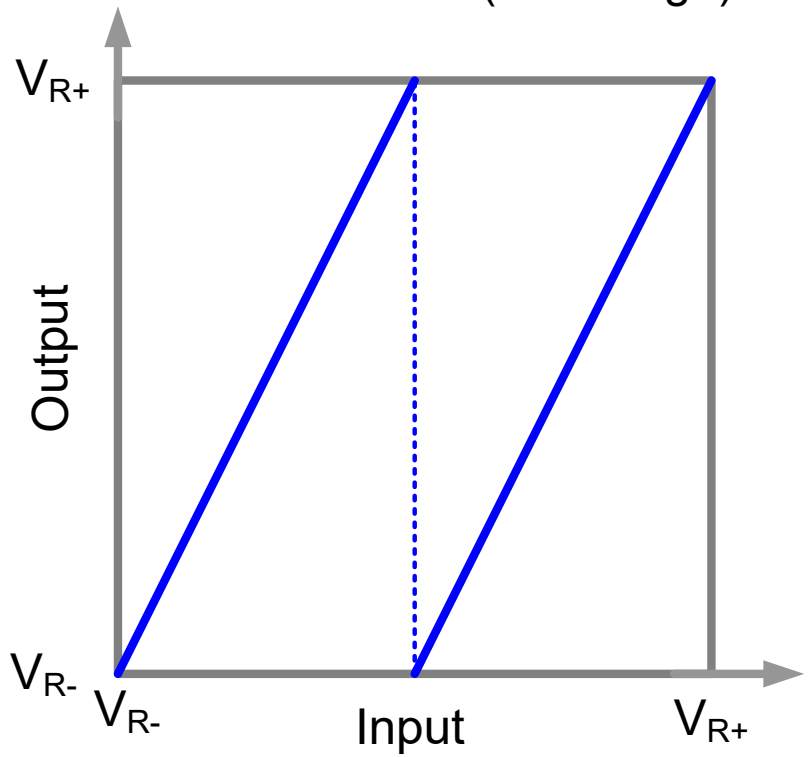


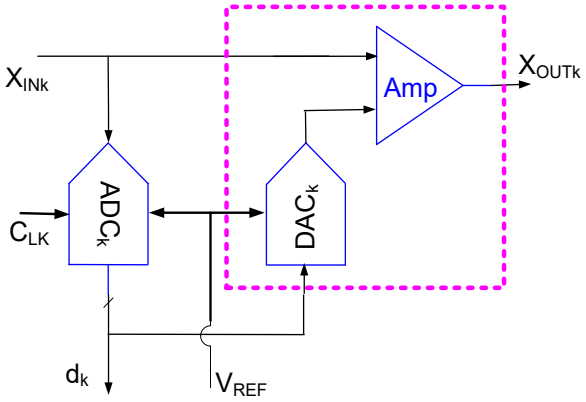




Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



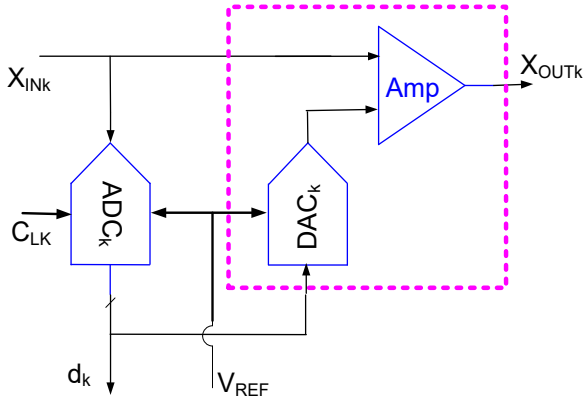


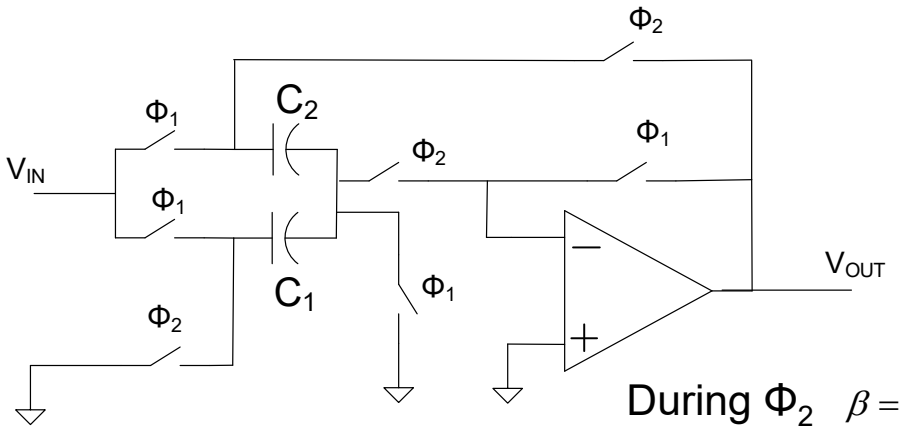
But what really happens?

Interstage Amplifiers

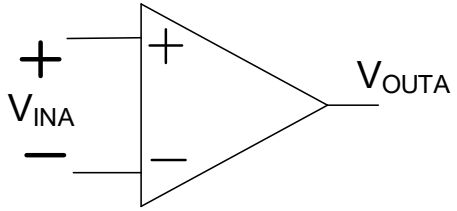
Ideal transfer characteristics (1 bit/stage)

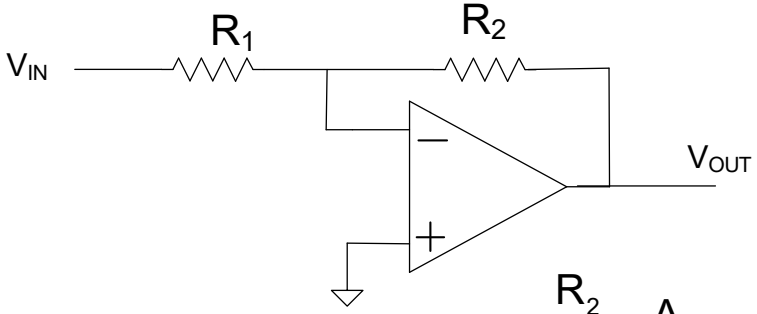
But what really happens?





During Φ_2 $\beta = \dfrac{C_2}{C_1 + C_2}$





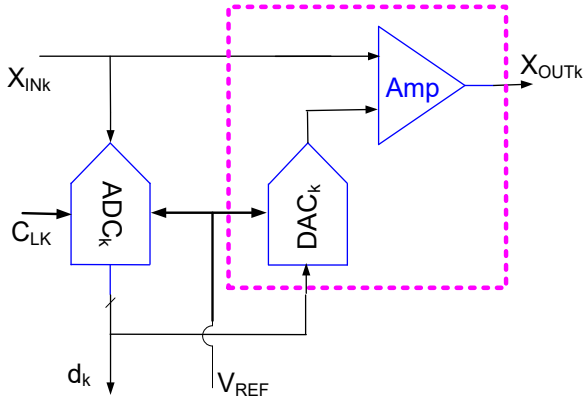
$$\beta = \frac{R_1}{R_1 + R_2}$$

$$A_{FB} = \frac{-\frac{R_2}{R_1 + R_2} A}{1 + A\frac{R_1}{R_1 + R_2}} = \frac{-\theta A}{1 + A\beta} = \frac{-\frac{R_2}{R_1} A\beta}{1 + A\beta}$$

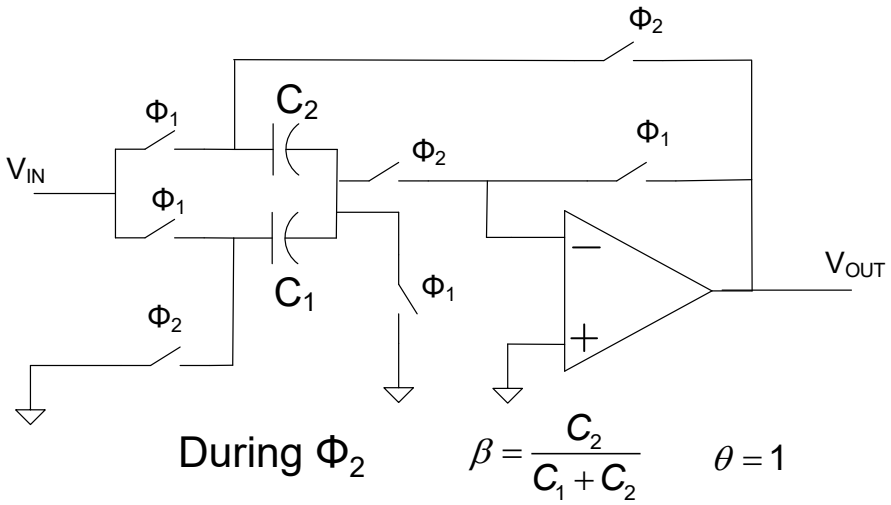
$$A_{FB} = \frac{\theta A}{1 + A\beta} \underset{|A| \neq \infty}{\neq} \frac{\theta}{\beta}$$

Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)



But what really happens?



During Φ_2 $\quad \beta = \frac{C_2}{C_1 + C_2}$ $\quad \theta = 1$

$$A_{FB} = \frac{\theta A}{1 + A\beta} \underset{|A| \neq \infty}{\neq} \frac{\theta}{\beta}$$

If ideally C_1=C_2 so that ideal gain is 2, will the actual gain be larger or smaller than 2?

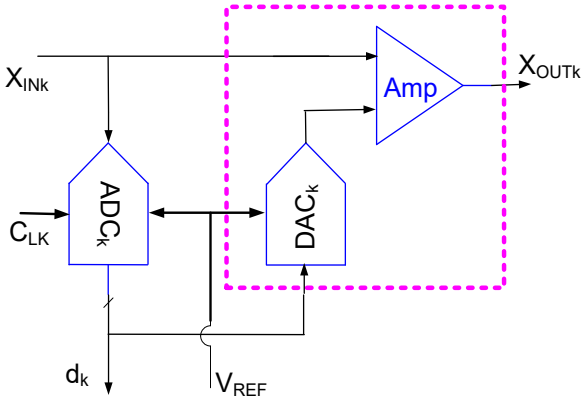
Depends:

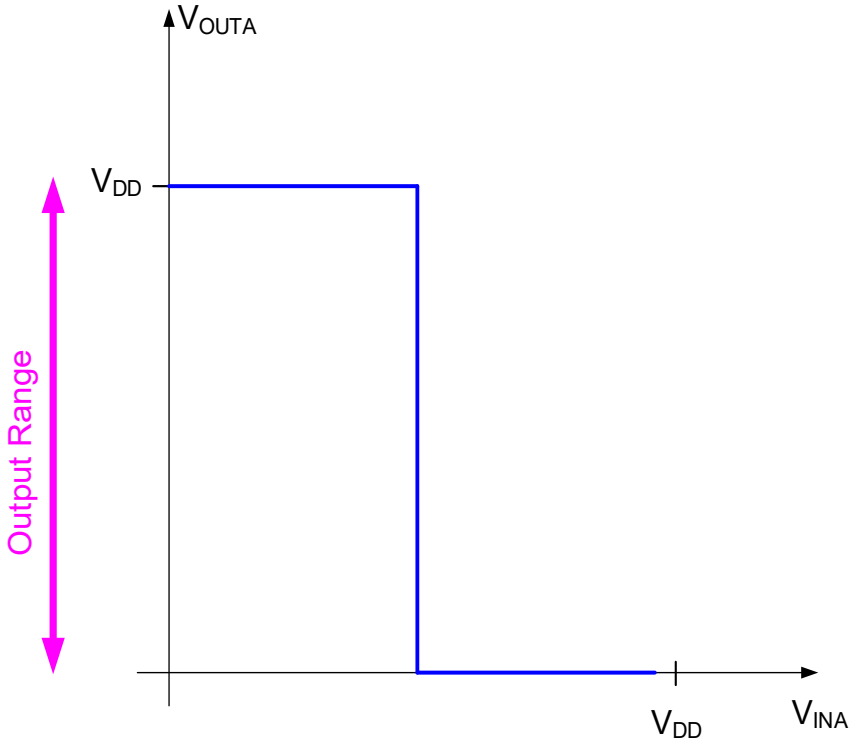
- Finite gain of Op Amp tends to make actual gain < 2
- Capacitor mismatch could make gain larger or smaller than 2
- For reasonable gain in Op Amp, mismatch effects likely will dominate

Interstage Amplifiers

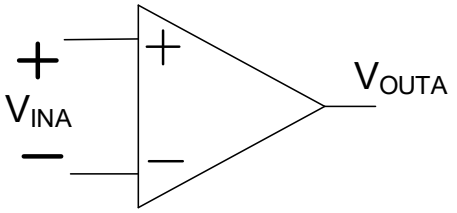
Ideal transfer characteristics (1 bit/stage)

But what really happens?





Ideal Op Amp Transfer Characteristics

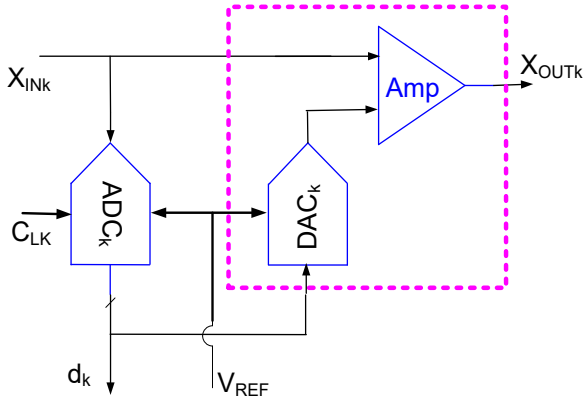


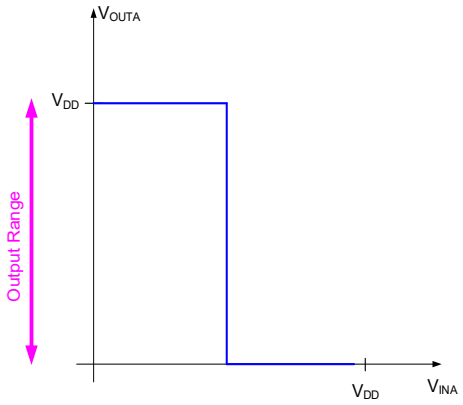
Op Amp (not Amp above)

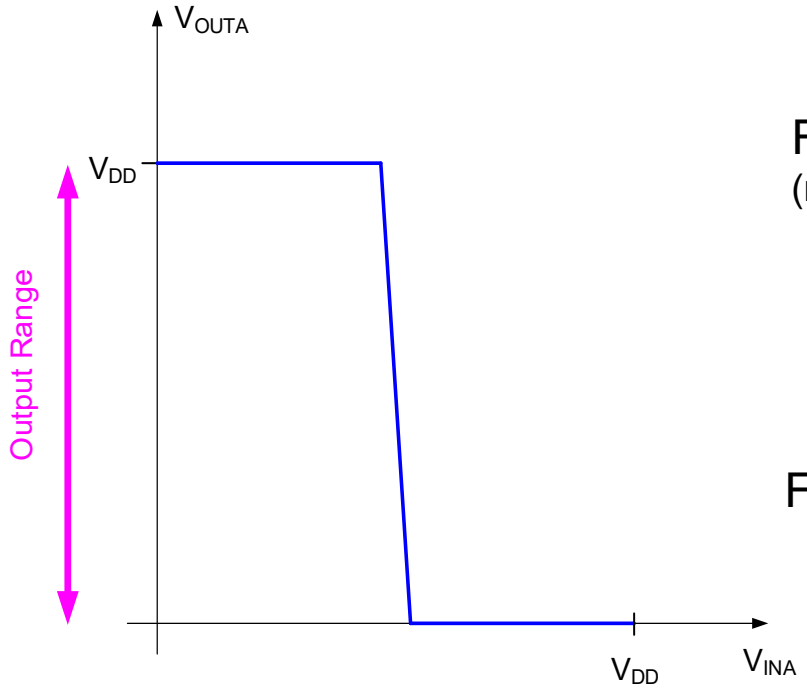
Interstage Amplifiers

Ideal transfer characteristics (1 bit/stage)

But what really happens?







For general FB amplifier
(not that in pipelined stage)

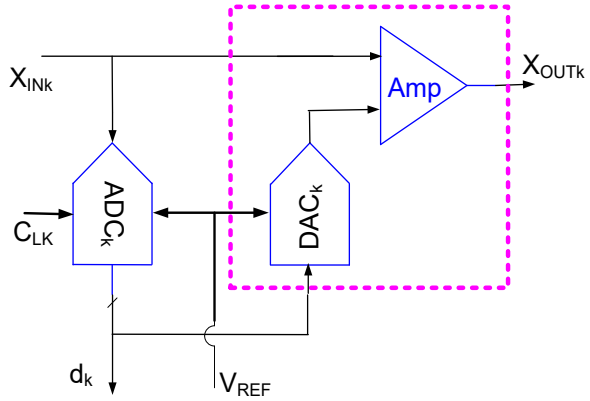
$$A_{FB} = \frac{A}{1+A\beta} \neq \frac{1}{\beta}$$

For FB amplifier in pipeline

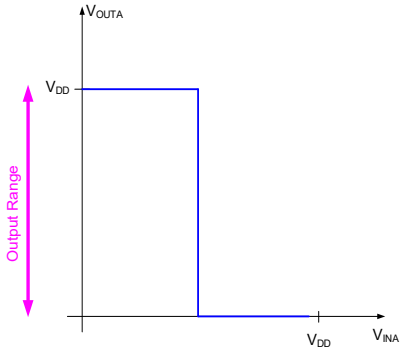
$$A_{FB} = \frac{\theta A}{1+A\beta} \underset{|A|\neq\infty}{\neq} \frac{\theta}{\beta}$$

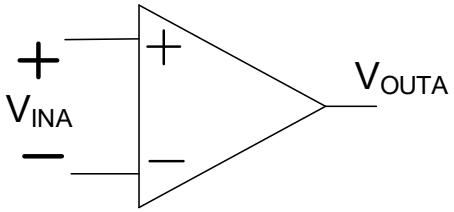
Interstage Amplifiers

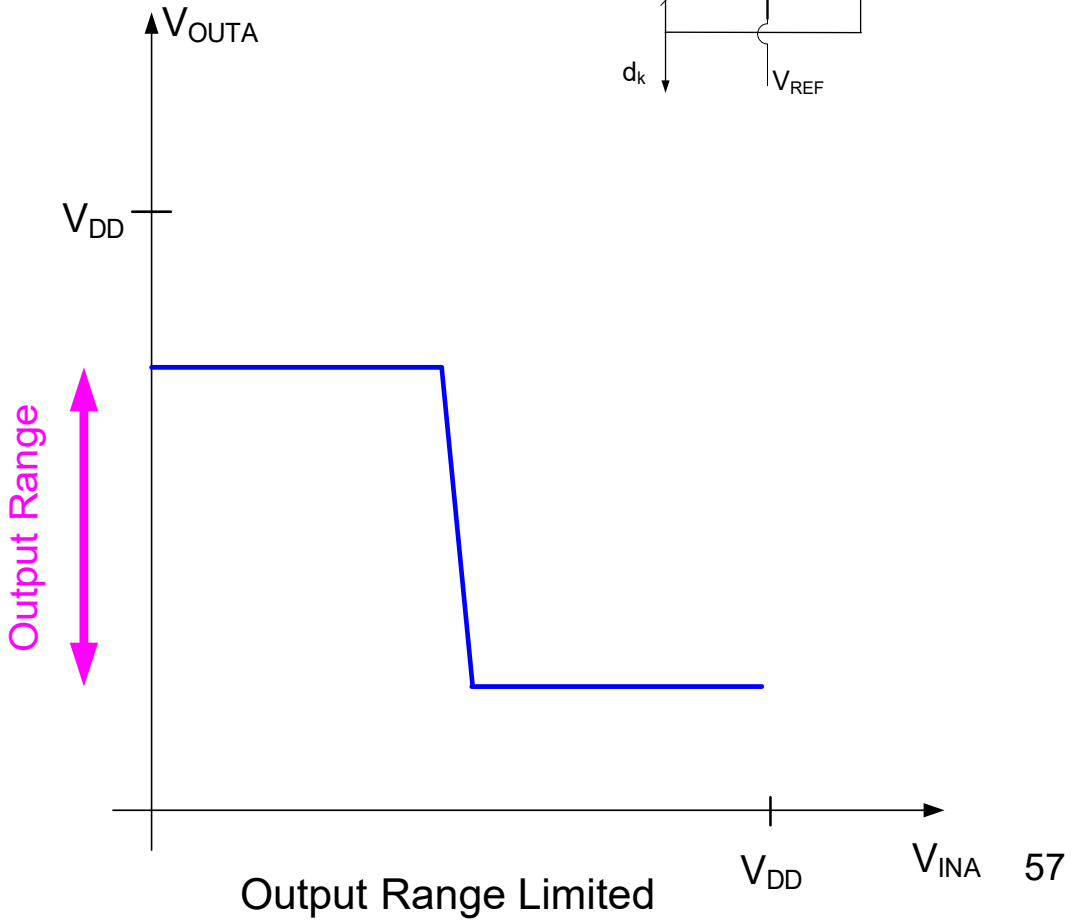
Ideal transfer characteristics (1 bit/stage)



But what really happens?

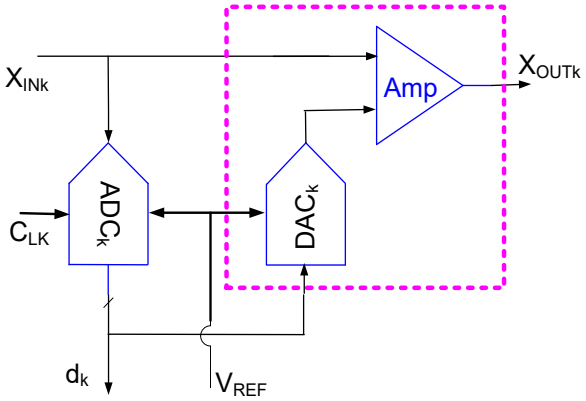




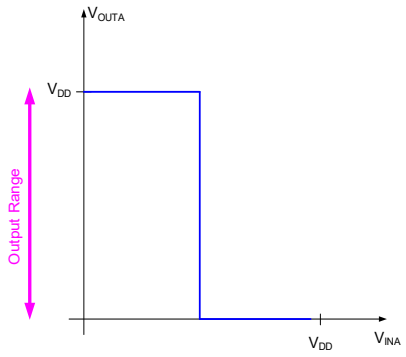


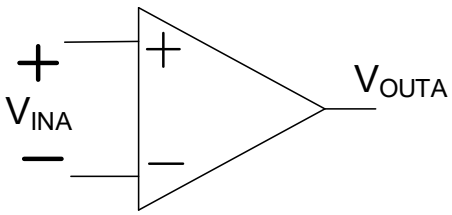
Interstage Amplifiers

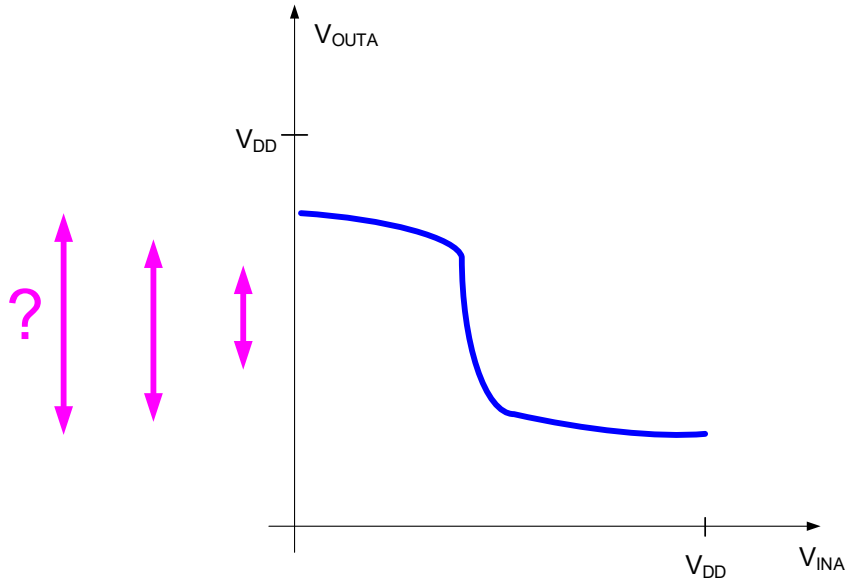
Ideal transfer characteristics (1 bit/stage)



But what really happens?







Output Range Limited and Transfer Characteristics are Nonlinear

Stay Safe and Stay Healthy !

End of Lecture 22